



PCA9635

16-bit Fm+ I²C-bus LED driver

Rev. 02 — 7 August 2006

Objective data sheet

1. General description

The PCA9635 is an I²C-bus controlled 16-bit LED driver optimized for Red/Green/Blue/Amber (RGBA) color mixing applications. Each LED output has its own 8-bit resolution (256 steps) fixed frequency individual PWM controller that operates at 97 kHz with a duty cycle that is adjustable from 0 % to 99.6 % to allow the LED to be set to a specific brightness value. An additional 8-bit resolution (256 steps) group PWM controller has both a fixed frequency of 190 Hz and an adjustable frequency between 24 Hz to once every 10.73 seconds with a duty cycle that is adjustable from 0 % to 99.6 % that is used to either dim or blink all LEDs with the same value.

Each LED output can be off, on (no PWM control), set at its individual PWM controller value or at both individual and group PWM controller values. The LED output driver is programmed to be either open-drain with a 25 mA current sink capability at 5 V or totem-pole with a 25 mA sink, 10 mA source capability at 5 V. The PCA9635 operates with a supply voltage range of 2.3 V to 5.5 V and the outputs are 5.5 V tolerant. LEDs can be directly connected to the LED output (up to 25 mA, 5.5 V) or controlled with external drivers and a minimum amount of discrete components for larger current LEDs or higher voltage LED strings.

The PCA9635 is one of the first LED controller devices in a new Fast-mode Plus (Fm+) family. Fm+ devices offer higher frequency (up to 1 MHz) and longer, more densely populated bus operation (up to 4000 pF).

The active LOW Output Enable input pin (\overline{OE}) allows asynchronous control of the LED outputs and can be used to set all the outputs to a defined I²C-bus programmable logic state. The \overline{OE} can also be used to externally PWM the outputs, which is useful when multiple devices need to be dimmed or blinked together using software control.

Software programmable LED Group and three Sub Call I²C-bus addresses allow all or defined groups of PCA9635 devices to respond to a common I²C-bus address, allowing for example, all red LEDs to be turned on or off at the same time or marquee chasing effect, thus minimizing I²C-bus commands. Seven hardware address pins allow up to 126 devices on the same bus.

The Software Reset (SWRST) Call allows the master to perform a reset of the PCA9635 through the I²C-bus, identical to the Power-On Reset (POR) that initializes the registers to their default state causing the outputs to be set HIGH (LED off). This allows an easy and quick way to reconfigure all device registers to the same condition.

PHILIPS

2. Features

- 16 LED drivers. Each output programmable at:
 - ◆ Off
 - ◆ On
 - ◆ Programmable LED brightness
 - ◆ Programmable group dimming/blinking mixed with individual LED brightness
- 1 MHz Fast-mode Plus compatible I²C-bus interface with 30 mA high drive capability on SDA output for driving high capacitive buses
- 256-step (8-bit) linear programmable brightness per LED output varying from fully off (default) to maximum brightness using a 97 kHz PWM signal
- 256-step group brightness control allows general dimming (using a 190 Hz PWM signal) from fully off to maximum brightness (default)
- 256-step group blinking with frequency programmable from 24 Hz to 10.73 s and duty cycle from 0 % to 99.6 %
- Sixteen totem-pole outputs (sink 25 mA and source 10 mA at 5 V) with software programmable open-drain LED outputs selection (default at totem-pole). No input function.
- Output state change programmable on the Acknowledge or the STOP Command to update outputs byte-by-byte or all at the same time (default to 'Change on STOP').
- Active LOW Output Enable (\overline{OE}) input pin. LED outputs programmable to logic 1, logic 0 or 'high-impedance' (default at power-up) when \overline{OE} is HIGH, thus allowing hardware blinking and dimming of the LEDs.
- 7 hardware address pins allow 126 PCA9635 devices to be connected to the same I²C-bus
- 4 software programmable I²C-bus addresses (one LED Group Call address and three LED Sub Call addresses) allow groups of devices to be addressed at the same time in any combination (for example, one register used for 'All Call' so that all the PCA9635s on the I²C-bus can be addressed at the same time and the second register used for three different addresses so that $\frac{1}{3}$ of all devices on the bus can be addressed at the same time in a group). Software enable and disable for I²C-bus address.
- Software Reset feature (SWRST Call) allows the device to be reset through the I²C-bus
- Up to 126 possible hardware adjustable individual I²C-bus addresses per device so that each device can be programmed individually.
- 25 MHz internal oscillator requires no external components
- Internal power-on reset
- Noise filter on SDA/SCL inputs
- Edge rate control on outputs
- No glitch on power-up
- Supports hot insertion
- Low standby current
- Operating power supply voltage range of 2.3 V to 5.5 V
- 5.5 V tolerant inputs
- -40 °C to +85 °C operation
- ESD protection exceeds 2000 V HBM per JESD22-A114, 200 V MM per JESD22-A115 and 1000 V CDM per JESD22-C101

- Latch-up testing is done to JEDEC Standard JESD78 which exceeds 100 mA
- Package offered: TSSOP28

3. Applications

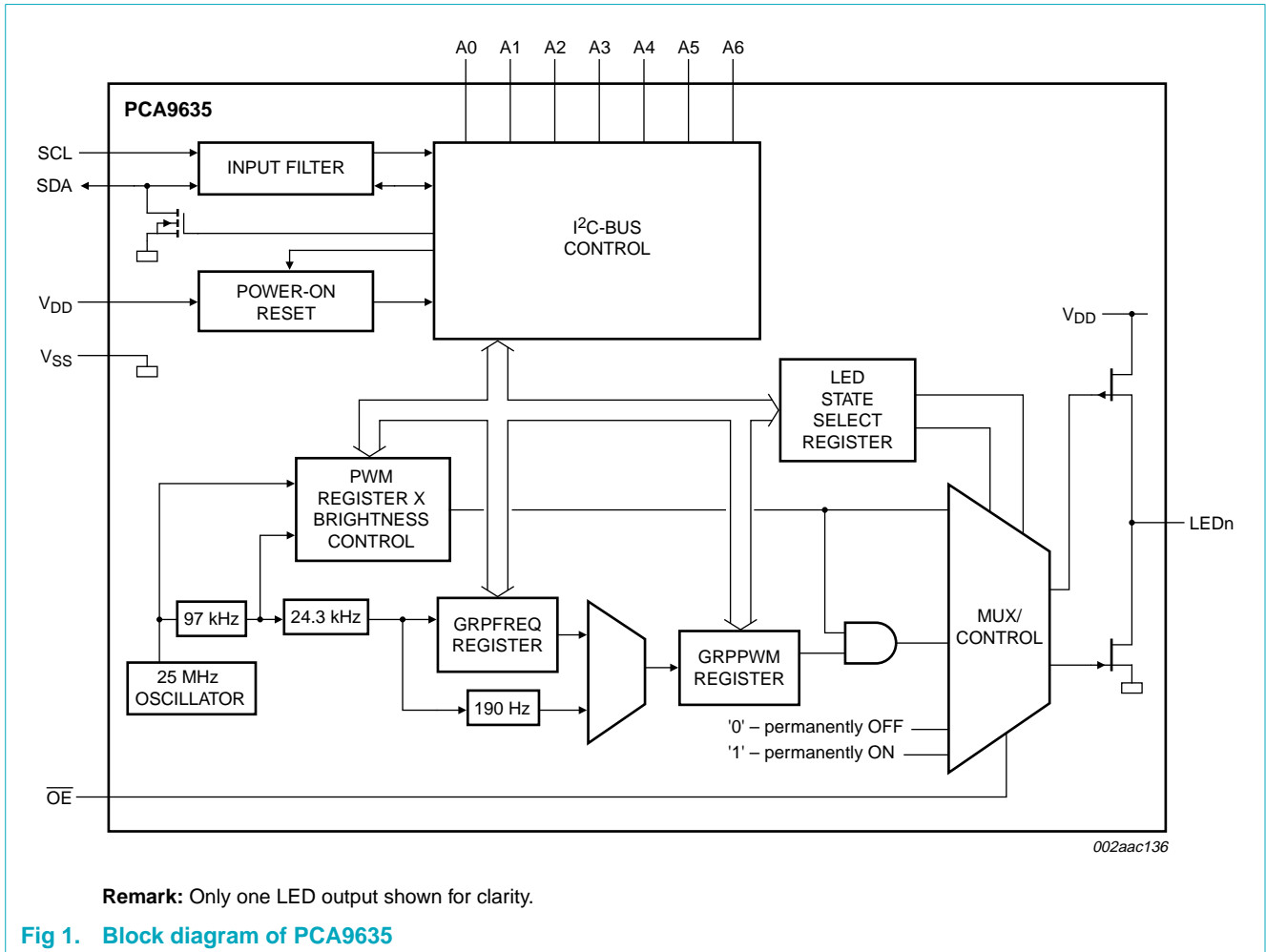
- RGB or RGBA LED drivers
- Decorative LED lighting
- LED status information
- LED displays
- LCD backlights
- Keypad backlights for cellular phones or handheld devices

4. Ordering information

Table 1. Ordering information

Type number	Topside mark	Package		
		Name	Description	Version
PCA9635PW	PCA9635PW	TSSOP28	plastic thin shrink small outline package; 28 leads; body width 4.4 mm	SOT361-1

5. Block diagram



6. Pinning information

6.1 Pinning

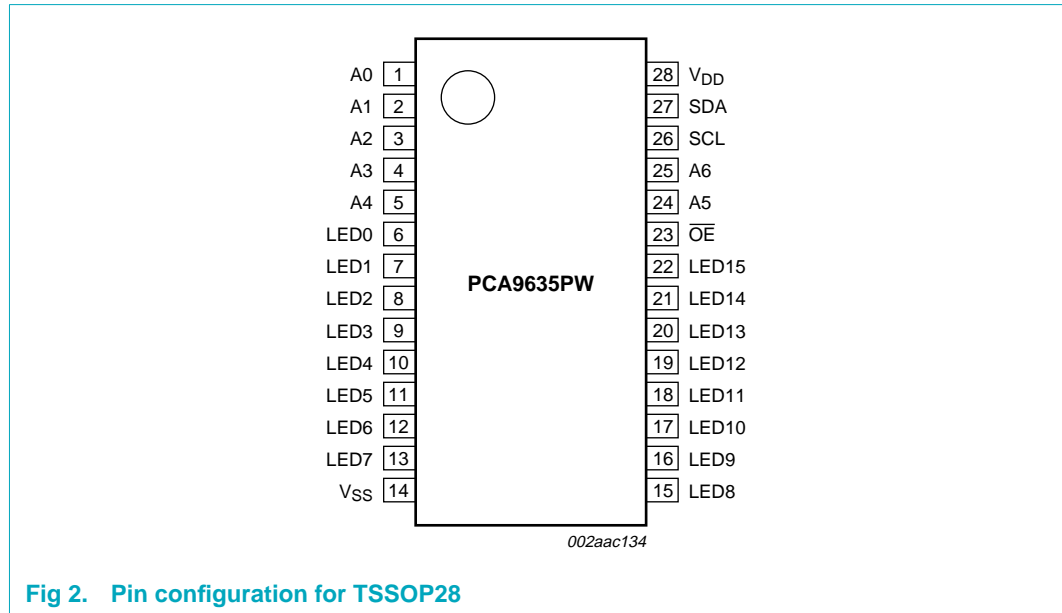


Fig 2. Pin configuration for TSSOP28

6.2 Pin description

Table 2. Pin description for TSSOP28

Symbol	Pin	Type	Description
A0	1	I	address input 0
A1	2	I	address input 1
A2	3	I	address input 2
A3	4	I	address input 3
A4	5	I	address input 4
LED0	6	O	LED driver 0
LED1	7	O	LED driver 1
LED2	8	O	LED driver 2
LED3	9	O	LED driver 3
LED4	10	O	LED driver 4
LED5	11	O	LED driver 5
LED6	12	O	LED driver 6
LED7	13	O	LED driver 7
V _{SS}	14	power supply	supply ground
LED8	15	O	LED driver 8
LED9	16	O	LED driver 9
LED10	17	O	LED driver 10
LED11	18	O	LED driver 11
LED12	19	O	LED driver 0

Table 2. Pin description for TSSOP28 ...continued

Symbol	Pin	Type	Description
LED13	20	O	LED driver 1
LED14	21	O	LED driver 2
LED15	22	O	LED driver 3
\overline{OE}	23	I	active LOW output enable
A5	24	I	address input 5
A6	25	I	address input 6
SCL	26	I	serial clock line
SDA	27	I/O	serial data line
V _{DD}	28	power supply	supply voltage

7. Functional description

Refer to [Figure 1 “Block diagram of PCA9635”](#).

7.1 Device addresses

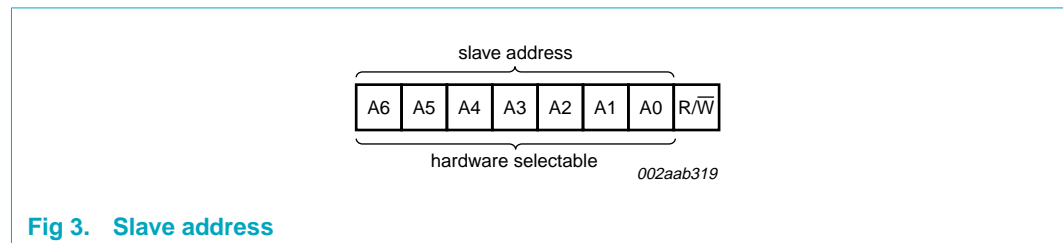
Following a START condition, the bus master must output the address of the slave it is accessing.

7.1.1 Regular I²C-bus slave address

The I²C-bus slave address of the PCA9635 is shown in [Figure 3](#). To conserve power, no internal pull-up resistors are incorporated on the hardware selectable address pins and they must be pulled HIGH or LOW.

Remark: Reserved I²C-bus addresses must be used with caution since they can interfere with:

- ‘reserved for future use’ I²C-bus addresses (0000 011, 1111 1XX)
- slave devices that use the 10-bit addressing scheme (1111 0XX)
- slave devices that are designed to respond to the General Call address (0000 000)
- High-speed mode (Hs-mode) master code (0000 1XX)



The last bit of the address byte defines the operation to be performed. When set to logic 1 a read is selected, while a logic 0 selects a write operation.

7.1.2 LED All Call I²C-bus address

- Default power-up value (ALLCALLADR register): E0h or 1110 000
- Programmable through I²C-bus (volatile programming)
- At power-up, LED All Call I²C-bus address is enabled. PCA9635 sends an ACK when E0h ($R/\overline{W} = 0$) or E1h ($R/\overline{W} = 1$) is sent by the master.

See [Section 7.3.8 “ALLCALLADR, LED All Call I²C-bus address”](#) for more detail.

Remark: The default LED All Call I²C-bus address (E0h or 1110 000) must not be used as a regular I²C-bus slave address since this address is enabled at power-up. All the PCA9635s on the I²C-bus will acknowledge the address if sent by the I²C-bus master.

7.1.3 LED Sub Call I²C-bus addresses

- 3 different I²C-bus addresses can be used
- Default power-up values:
 - SUBADR1 register: E2h or 1110 001
 - SUBADR2 register: E4h or 1110 010
 - SUBADR3 register: E8h or 1110 100
- Programmable through I²C-bus (volatile programming)
- At power-up, Sub Call I²C-bus addresses are disabled. PCA9635 does not send an ACK when E2h ($R/\overline{W} = 0$) or E3h ($R/\overline{W} = 1$), E4h ($R/\overline{W} = 0$) or E5h ($R/\overline{W} = 1$), or E8h ($R/\overline{W} = 0$) or E9h ($R/\overline{W} = 1$) is sent by the master.

See [Section 7.3.7 “SUBADR1 to SUBADR3, I²C-bus subaddress 1 to 3”](#) for more detail.

Remark: The default LED Sub Call I²C-bus addresses may be used as regular I²C-bus slave addresses as long as they are disabled.

7.1.4 Software Reset I²C-bus address

The address shown in [Figure 4](#) is used when a reset of the PCA9635 needs to be performed by the master. The Software Reset address (SWRST Call) must be used with $R/\overline{W} = 0$. If $R/\overline{W} = 1$, the PCA9635 does not acknowledge the SWRST. See [Section 7.6 “Software Reset”](#) for more detail.

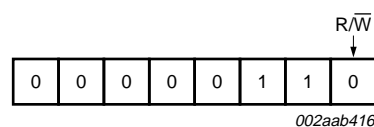


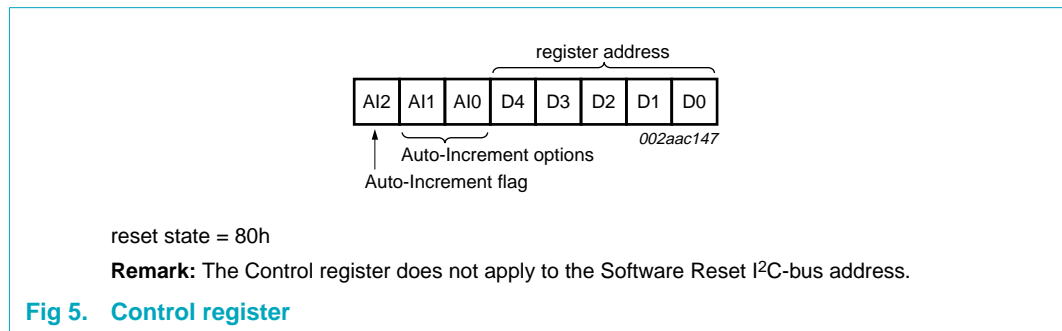
Fig 4. Software Reset address

Remark: The Software Reset I²C-bus address is a reserved address and cannot be used as a regular I²C-bus slave address or as an LED All Call or LED Sub Call address.

7.2 Control register

Following the successful acknowledgement of the slave address, LED All Call address or LED Sub Call address, the bus master will send a byte to the PCA9635, which will be stored in the Control register.

The lowest 5 bits are used as a pointer to determine which register will be accessed (D[4:0]). The highest 3 bits are used as Auto-Increment flag and Auto-Increment options (AI[2:0]).



When the Auto-Increment flag is set (AI2 = logic 1), the five low order bits of the Control register are automatically incremented after a read or write. This allows the user to program the registers sequentially. Four different types of Auto-Increment are possible, depending on AI1 and AI0 values.

Table 3. Auto-Increment options

AI2	AI1	AI0	Function
0	0	0	no Auto-Increment
1	0	0	Auto-Increment for all registers. D[4:0] roll over to '0 0000' after the last register (1 1011) is accessed.
1	0	1	Auto-Increment for individual brightness registers only. D[4:0] roll over to '0 0010' after the last register (1 0001) is accessed.
1	1	0	Auto-Increment for global control registers only. D[4:0] roll over to '1 0010' after the last register (1 0011) is accessed.
1	1	1	Auto-Increment for individual and global control registers only. D[4:0] roll over to '0 0010' after the last register (1 0011) is accessed.

Remark: Other combinations not shown in [Table 3](#) (AI[2:0] = 001, 010, and 011) are reserved and must not be used for proper device operation.

AI[2:0] = 000 is used when the same register must be accessed several times during a single I²C-bus communication, for example, changes the brightness of a single LED. Data is overwritten each time the register is accessed during a write operation.

AI[2:0] = 100 is used when all the registers must be sequentially accessed, for example, power-up programming.

AI[2:0] = 101 is used when the four LED drivers must be individually programmed with different values during the same I²C-bus communication, for example, changing color setting to another color setting.

AI[2:0] = 110 is used when the LED drivers must be globally programmed with different settings during the same I²C-bus communication, for example, global brightness or blinking change.

AI[2:0] = 111 is used when individual and global changes must be performed during the same I²C-bus communication, for example, changing a color and global brightness at the same time.

Only the 5 least significant bits D[4:0] are affected by the AI[2:0] bits.

When the Control register is written, the register entry point determined by D[4:0] is the first register that will be addressed (read or write operation), and can be anywhere between 0 0000 and 1 1011 (as defined in [Table 4](#)). When AI[2] = 1, the Auto-Increment flag is set and the rollover value at which the point where the register increment stops and goes to the next one is determined by AI[2:0]. See [Table 3](#) for rollover values. For example, if the Control register = 1111 0100 (F4h), then the register addressing sequence will be (in hex):

14 → ... → 1B → 00 → ... → 13 → 02 → ... → 13 → 02 → ... → 13 → 02 → ... as long as the master keeps sending or reading data.

7.3 Register definitions

Table 4. Register summary^{[1][2]}

Register number (hex)	D4	D3	D2	D1	D0	Name	Type	Function
00	0	0	0	0	0	MODE1	read/write	Mode register 1
01	0	0	0	0	1	MODE2	read/write	Mode register 2
02	0	0	0	1	0	PWM0	read/write	brightness control LED0
03	0	0	0	1	1	PWM1	read/write	brightness control LED1
04	0	0	1	0	0	PWM2	read/write	brightness control LED2
05	0	0	1	0	1	PWM3	read/write	brightness control LED3
06	0	0	1	1	0	PWM4	read/write	brightness control LED4
07	0	0	1	1	1	PWM5	read/write	brightness control LED5
08	0	1	0	0	0	PWM6	read/write	brightness control LED6
09	0	1	0	0	1	PWM7	read/write	brightness control LED7
0A	0	1	0	1	0	PWM8	read/write	brightness control LED8
0B	0	1	0	1	1	PWM9	read/write	brightness control LED9
0C	0	1	1	0	0	PWM10	read/write	brightness control LED10
0D	0	1	1	0	1	PWM11	read/write	brightness control LED11
0E	0	1	1	1	0	PWM12	read/write	brightness control LED12
0F	0	1	1	1	1	PWM13	read/write	brightness control LED13
10	1	0	0	0	0	PWM14	read/write	brightness control LED14
11	1	0	0	0	1	PWM15	read/write	brightness control LED15
12	1	0	0	1	0	GRPPWM	read/write	group duty cycle control
13	1	0	0	1	1	GRPFREQ	read/write	group frequency

Table 4. Register summary^{[1][2]} ...continued

Register number (hex)	D4	D3	D2	D1	D0	Name	Type	Function
14	1	0	1	0	0	LEDOUT0	read/write	LED output state 0
15	1	0	1	0	1	LEDOUT1	read/write	LED output state 1
16	1	0	1	1	0	LEDOUT2	read/write	LED output state 2
17	1	0	1	1	1	LEDOUT3	read/write	LED output state 3
18	1	1	0	0	0	SUBADR1	read/write	I ² C-bus subaddress 1
19	1	1	0	0	1	SUBADR2	read/write	I ² C-bus subaddress 2
1A	1	1	0	1	0	SUBADR3	read/write	I ² C-bus subaddress 3
1B	1	1	0	1	1	ALLCALLADR	read/write	LED All Call I ² C-bus address

[1] Only D[4:0] = 0 0000 to 1 1011 are allowed and will be acknowledged. D[4:0] = 1 1100 to 1 1111 are reserved and will not be acknowledged.

[2] When writing to the Control register, bit 4 must be programmed with logic 0 for proper device operation.

7.3.1 Mode register 1, MODE1

Table 5. MODE1 - Mode register 1 (address 00h) bit description

Legend: * default value

Bit	Symbol	Access	Value	Description
7	AI2	read only	0	Register Auto-Increment disabled
			1*	Register Auto-Increment enabled
6	AI1	read only	0*	Auto-Increment bit 1 = 0
			1	Auto-Increment bit 1 = 1
5	AI0	read only	0*	Auto-Increment bit 0 = 0
			1	Auto-Increment bit 0 = 1
4	SLEEP	R/W	0	Normal mode ^[1] .
			1*	Low power mode. Oscillator off ^[2] .
3	SUB1	R/W	0*	PCA9635 does not respond to I ² C-bus subaddress 1.
			1	PCA9635 responds to I ² C-bus subaddress 1.
2	SUB2	R/W	0*	PCA9635 does not respond to I ² C-bus subaddress 2.
			1	PCA9635 responds to I ² C-bus subaddress 2.
1	SUB3	R/W	0*	PCA9635 does not respond to I ² C-bus subaddress 3.
			1	PCA9635 responds to I ² C-bus subaddress 3.
0	ALLCALL	R/W	0	PCA9635 does not respond to LED All Call I ² C-bus address.
			1*	PCA9635 responds to LED All Call I ² C-bus address.

[1] It takes 500 μ s max. for the oscillator to be up and running once SLEEP bit has been set to logic 1. Timings on LEDn outputs are not guaranteed if PWMx, GRPPWM or GRPFREQ registers are accessed within the 500 μ s window.

[2] No blinking or dimming is possible when the oscillator is off.

7.3.2 Mode register 2, MODE2

Table 6. MODE2 - Mode register 2 (address 01h) bit description

Legend: * default value

Bit	Symbol	Access	Value	Description
7	-	read only	0*	reserved
6	-	read only	0*	reserved
5	DMBLNK	R/W	0*	group control = dimming
			1	group control = blinking
4	INVRT ^[1]	R/W	0*	Output logic state not inverted. Value to use when no external driver used. Applicable when $\overline{OE} = 0$.
			1	Output logic state inverted. Value to use when external driver used. Applicable when $\overline{OE} = 0$.
3	OCH	R/W	0*	Outputs change on STOP command. ^[2]
			1	Outputs change on ACK.
2	OUTDRV ^[1]	R/W	0	The 16 LED outputs are configured with an open-drain structure.
			1*	The 16 LED outputs are configured with a totem-pole structure.
1 to 0	OUTNE[1:0] ^[3]	R/W	00	When $\overline{OE} = 1$ (output drivers not enabled), LEDn = 0.
			01*	When $\overline{OE} = 1$ (output drivers not enabled): LEDn = 1 when OUTDRV = 1 LEDn = high-impedance when OUTDRV = 0 (same as OUTNE[1:0] = 10)
			10	When $\overline{OE} = 1$ (output drivers not enabled), LEDn = high-impedance.
			11	reserved

[1] See [Section 7.7 “Using the PCA9635 with and without external drivers”](#) for more details.

[2] Change of the outputs at the STOP command allows synchronizing outputs of more than one PCA9635. Applicable to registers from 02h (PWM0) to 08h (LEDOUT) only.

[3] See [Section 7.4 “Active LOW output enable input”](#) for more details.

7.3.3 PWM0 to PWM15, individual brightness control

Table 7. PWM0 to PWM15 - PWM registers 0 to 15 (address 02h to 11h) bit description

Legend: * default value

Address	Register	Bit	Symbol	Access	Value	Description
02h	PWM0	7:0	IDC0[7:0]	R/W	0000 0000*	PWM0 Individual Duty Cycle
03h	PWM1	7:0	IDC1[7:0]	R/W	0000 0000*	PWM1 Individual Duty Cycle
04h	PWM2	7:0	IDC2[7:0]	R/W	0000 0000*	PWM2 Individual Duty Cycle
05h	PWM3	7:0	IDC3[7:0]	R/W	0000 0000*	PWM3 Individual Duty Cycle
06h	PWM4	7:0	IDC4[7:0]	R/W	0000 0000*	PWM4 Individual Duty Cycle
07h	PWM5	7:0	IDC5[7:0]	R/W	0000 0000*	PWM5 Individual Duty Cycle
08h	PWM6	7:0	IDC6[7:0]	R/W	0000 0000*	PWM6 Individual Duty Cycle
09h	PWM7	7:0	IDC7[7:0]	R/W	0000 0000*	PWM7 Individual Duty Cycle
0Ah	PWM8	7:0	IDC8[7:0]	R/W	0000 0000*	PWM8 Individual Duty Cycle
0Bh	PWM9	7:0	IDC9[7:0]	R/W	0000 0000*	PWM9 Individual Duty Cycle
0Ch	PWM10	7:0	IDC10[7:0]	R/W	0000 0000*	PWM10 Individual Duty Cycle
0Dh	PWM11	7:0	IDC11[7:0]	R/W	0000 0000*	PWM11 Individual Duty Cycle
0Eh	PWM12	7:0	IDC12[7:0]	R/W	0000 0000*	PWM12 Individual Duty Cycle

Table 7. PWM0 to PWM15 - PWM registers 0 to 15 (address 02h to 11h) bit description
...continued

Address	Register	Bit	Symbol	Access	Value	Description
0Fh	PWM13	7:0	IDC13[7:0]	R/W	0000 0000*	PWM13 Individual Duty Cycle
10h	PWM14	7:0	IDC14[7:0]	R/W	0000 0000*	PWM14 Individual Duty Cycle
11h	PWM15	7:0	IDC15[7:0]	R/W	0000 0000*	PWM15 Individual Duty Cycle

A 97 kHz fixed frequency signal is used for each output. Duty cycle is controlled through 256 linear steps from 00h (0 % duty cycle = LED output off) to FFh (99.6 % duty cycle = LED output at maximum brightness). Applicable to LED outputs programmed with LDRx = 10 or 11 (LEDOUT0 to LEDOUT3 registers).

$$duty\ cycle = \frac{IDC_x[7:0]}{256}$$

7.3.4 GRPPWM, group duty cycle control

Table 8. GRPPWM - Group brightness control register (address 12h) bit description
Legend: * default value

Address	Register	Bit	Symbol	Access	Value	Description
12h	GRPPWM	7:0	GDC[7:0]	R/W	1111 1111	GRPPWM register

When DMBLNK bit (MODE2 register) is programmed with logic 0, a 190 Hz fixed frequency signal is superimposed with the 97 kHz individual brightness control signal. GRPPWM is then used as a global brightness control allowing the LED outputs to be dimmed with the same value. The value in GRPFREQ is then a 'Don't care'.

General brightness for the 16 outputs is controlled through 256 linear steps from 00h (0 % duty cycle = LED output off) to FFh (99.6 % duty cycle = maximum brightness). Applicable to LED outputs programmed with LDRx = 11 (LEDOUT0 to LEDOUT3 registers).

When DMBLNK bit is programmed with logic 1, GRPPWM and GRPFREQ registers define a global blinking pattern, where GRPFREQ contains the blinking period (from 24 Hz to 10.73 s) and GRPPWM the duty cycle (ON/OFF ratio in %).

$$duty\ cycle = \frac{GDC[7:0]}{256}$$

7.3.5 GRPFREQ, group frequency

Table 9. GRPFREQ - Group Frequency register (address 13h) bit description
Legend: * default value

Address	Register	Bit	Symbol	Access	Value	Description
13h	GRPFREQ	7:0	GFRQ[7:0]	R/W	0000 0000*	GRPFREQ register

GRPFREQ is used to program the global blinking period when DMBLNK bit (MODE2 register) is equal to 1. Value in this register is a 'Don't care' when DMBLNK = 0. Applicable to LED outputs programmed with LDRx = 11 (LEDOUT0 to LEDOUT3 registers).

Blinking period is controlled through 256 linear steps from 00h (41 ms, frequency 24 Hz) to FFh (10.73 s).

$$\text{global blinking period} = \frac{GFRQ[7:0] + 1}{24} \text{ (s)}$$

7.3.6 LEDOUT0 to LEDOUT3, LED driver output state

Table 10. LEDOUT0 to LEDOUT3 - LED driver output state register (address 14h to 17h) bit description

Legend: * default value

Address	Register	Bit	Symbol	Access	Value	Description
14h	LEDOUT0	7:6	LDR3	R/W	00*	LED3 output state control
		5:4	LDR2	R/W	00*	LED2 output state control
		3:2	LDR1	R/W	00*	LED1 output state control
		1:0	LDR0	R/W	00*	LED0 output state control
15h	LEDOUT1	7:6	LDR7	R/W	00*	LED7 output state control
		5:4	LDR6	R/W	00*	LED6 output state control
		3:2	LDR5	R/W	00*	LED5 output state control
		1:0	LDR4	R/W	00*	LED4 output state control
16h	LEDOUT2	7:6	LDR11	R/W	00*	LED11 output state control
		5:4	LDR10	R/W	00*	LED10 output state control
		3:2	LDR9	R/W	00*	LED9 output state control
		1:0	LDR8	R/W	00*	LED8 output state control
17h	LEDOUT3	7:6	LDR15	R/W	00*	LED15 output state control
		5:4	LDR14	R/W	00*	LED14 output state control
		3:2	LDR13	R/W	00*	LED13 output state control
		1:0	LDR12	R/W	00*	LED12 output state control

LDRx = 00 — LED driver x is off (default power-up state).

LDRx = 01 — LED driver x is fully on (individual brightness and group dimming/blinking not controlled).

LDRx = 10 — LED driver x individual brightness can be controlled through its PWMx register.

LDRx = 11 — LED driver x individual brightness and group dimming/blinking can be controlled through its PWMx register and the GRPPWM registers.

7.3.7 SUBADR1 to SUBADR3, I²C-bus subaddress 1 to 3

Table 11. SUBADR1 to SUBADR3 - I²C-bus subaddress registers 0 to 3 (address 18h to 1Ah) bit description

Legend: * default value

Address	Register	Bit	Symbol	Access	Value	Description
18h	SUBADR1	7:1	A1[7:1]	R/W	1110 001*	I ² C-bus subaddress 1
		0	A1[0]	R only	0*	reserved
19h	SUBADR2	7:1	A2[7:1]	R/W	1110 010*	I ² C-bus subaddress 2
		0	A2[0]	R only	0*	reserved
1Ah	SUBADR3	7:1	A3[7:1]	R/W	1110 100*	I ² C-bus subaddress 3
		0	A3[0]	R only	0*	reserved

Subaddresses are programmable through the I²C-bus. Default power-up values are E2h, E4h, E8h, and the device(s) will not acknowledge these addresses right after power-up (the corresponding SUBx bit in MODE1 register is equal to 0).

Once subaddresses have been programmed to their right values, SUBx bits need to be set to 1 in order to have the device acknowledging these addresses (MODE1 register).

Only the 7 MSBs representing the I²C-bus subaddress are valid. The LSB in SUBADR_x register is a read-only bit (0).

When SUBx is set to 1, the corresponding I²C-bus subaddress can be used during either an I²C-bus read or write sequence.

7.3.8 ALLCALLADR, LED All Call I²C-bus address

Table 12. ALLCALLADR - LED All Call I²C-bus address register (address 1Bh) bit description

Legend: * default value

Address	Register	Bit	Symbol	Access	Value	Description
1Bh	ALLCALLADR	7:1	AC[7:1]	R/W	1110 000*	ALLCALL I ² C-bus address register
		0	AC[0]	R only	0*	reserved

The LED All Call I²C-bus address allows all the PCA9635s in the bus to be programmed at the same time (ALLCALL bit in register MODE1 must be equal to 1 (power-up default state)). This address is programmable through the I²C-bus and can be used during either an I²C-bus read or write sequence. The register address can also be programmed as a Sub Call.

Only the 7 MSBs representing the All Call I²C-bus address are valid. The LSB in ALLCALLADR register is a read-only bit (0).

If ALLCALL bit = 0, the device does not acknowledge the address programmed in register ALLCALLADR.

7.4 Active LOW output enable input

The active LOW output enable (\overline{OE}) pin, allows to enable or disable all the LED outputs at the same time.

- When a LOW level is applied to \overline{OE} pin, all the LED outputs are enabled and follow the output state defined in the LEDOUT register with the polarity defined by INVRT bit (MODE2 register).
- When a HIGH level is applied to \overline{OE} pin, all the LED outputs are programmed to the value that is defined by OUTNE[1:0] in the MODE2 register.

Table 13. LED outputs when $\overline{OE} = 1$

OUTNE1	OUTNE0	LED outputs
0	0	0
0	1	1 if OUTDRV = 1, high-impedance if OUTDRV = 0
1	0	high-impedance
1	1	reserved

The \overline{OE} pin can be used as a synchronization signal to switch on/off several PCA9635 devices at the same time. This requires an external clock reference that provides blinking period and the duty cycle.

The \overline{OE} pin can also be used as an external dimming control signal. The frequency of the external clock must be high enough not to be seen by the human eye, and the duty cycle value determines the brightness of the LEDs.

Remark: Do not use \overline{OE} as an external blinking control signal when internal global blinking is selected (DMBLNK = 1, MODE2 register) since it will result in an undefined blinking pattern. Do not use \overline{OE} as an external dimming control signal when internal global dimming is selected (DMBLNK = 0, MODE2 register) since it will result in an undefined dimming pattern.

7.5 Power-on reset

When power is applied to V_{DD} , an internal power-on reset holds the PCA9635 in a reset condition until V_{DD} has reached V_{POR} . At this point, the reset condition is released and the PCA9635 registers and I²C-bus state machine are initialized to their default states (all zeroes) causing all the channels to be deselected. Thereafter, V_{DD} must be lowered below 0.2 V to reset the device.

7.6 Software Reset

The Software Reset Call (SWRST Call) allows all the devices in the I²C-bus to be reset to the power-up state value through a specific formatted I²C-bus command. To be performed correctly, it implies that the I²C-bus is functional and that there is no device hanging the bus.

The SWRST Call function is defined as the following:

1. A START command is sent by the I²C-bus master.
2. The reserved SWRST I²C-bus address '0000 011' with the R/W bit set to '0' (write) is sent by the I²C-bus master.
3. The PCA9635 device(s) acknowledge(s) after seeing the SWRST Call address '0000 0110' (06h) only. If the R/W bit is set to '1' (read), no acknowledge is returned to the I²C-bus master.
4. Once the SWRST Call address has been sent and acknowledged, the master sends 2 bytes with 2 specific values (SWRST data byte 1 and byte 2):
 - a. Byte 1 = A5h: the PCA9635 acknowledges this value only. If byte 1 is not equal to A5h, the PCA9635 does not acknowledge it.
 - b. Byte 2 = 5Ah: the PCA9635 acknowledges this value only. If byte 2 is not equal to 5Ah, then the PCA9635 does not acknowledge it.

If more than 2 bytes of data are sent, the PCA9635 does not acknowledge any more.

5. Once the right 2 bytes (SWRST data byte 1 and byte 2 only) have been sent and correctly acknowledged, the master sends a STOP command to end the SWRST Call: the PCA9635 then resets to the default value (power-up value) and is ready to be addressed again within the specified bus free time (t_{BUF}).

The I²C-bus master must interpret a non-acknowledge from the PCA9635 (at any time) as a 'SWRST Call Abort'. The PCA9635 does not initiate a reset of its registers. This happens only when the format of the SWRST Call sequence is not correct.

7.7 Using the PCA9635 with and without external drivers

The PCA9635 LED output drivers are 5.5 V only tolerant and can sink up to 25 mA at 5 V.

If the device needs to drive LEDs to a higher voltage and/or higher current, use of an external driver is required.

- INVRT bit (MODE2 register) can be used to keep the LED PWM control firmware the same (PWMx and GRPPWM values directly calculated from their respective formulas and the LED output state determined by LEDOUT register value) independently of the type of external driver. This bit allows LED output polarity inversion/non-inversion only when $\overline{OE} = 0$.
- OUTDRV bit (MODE2 register) allows minimizing the amount of external components required to control the external driver (N-type or P-type device).

Table 14. Use of INVRT and OUTDRV based on connection to the LEDn outputs when $\overline{OE} = 0$ ^[1]

INVRT	OUTDRV	Direct connection to LEDn		External N-type driver		External P-type driver	
		Firmware	External pull-up resistor	Firmware	External pull-up resistor	Firmware	External pull-up resistor
0	0	formulas and LED output state values apply ^[2]	LED current limiting R ^[2]	formulas and LED output state values inverted	required	formulas and LED output state values apply	required
0	1	formulas and LED output state values apply ^[2]	LED current limiting R ^[2]	formulas and LED output state values inverted	not required	formulas and LED output state values apply ^[4]	not required ^[4]
1	0	formulas and LED output state values inverted	LED current limiting R	formulas and LED output state values apply	required	formulas and LED output state values inverted	required
1	1	formulas and LED output state values inverted	LED current limiting R	formulas and LED output state values apply ^[3]	not required ^[3]	formulas and LED output state values inverted	not required

[1] When $\overline{OE} = 1$, LED output state is controlled only by OUTNE[1:0] bits (MODE2 register).

[2] Correct configuration when LEDs directly connected to the LEDn outputs (connection to V_{DD} through current limiting resistor).

[3] Optimum configuration when external N-type (NPN, NMOS) driver used.

[4] Optimum configuration when external P-type (PNP, PMOS) driver used.

Table 15. Output transistors based on LEDOUT registers, INVRT and OUTDRV bits when $\overline{OE} = 0$ ^[1]

LEDOUT	INVRT	OUTDRV	Upper transistor (V _{DD} to LEDn)	Lower transistor (LEDn to V _{SS})	LEDn state
00 LED driver off	0	0	off	off	high-Z ^[2]
	0	1	on	off	V _{DD}
	1	0	off	on	V _{SS}
	1	1	off	on	V _{SS}
01 LED driver on	0	0	off	on	V _{SS}
	0	1	off	on	V _{SS}
	1	0	off	off	high-Z ^[2]
	1	1	on	off	V _{DD}
10 Individual brightness control	0	0	off	individual PWM (non-inverted)	V _{SS} /high-Z ^[2] = PWMx value
	0	1	individual PWM (non-inverted)	individual PWM (non-inverted)	V _{SS} /V _{DD} = PWMx value
	1	0	off	individual PWM (inverted)	high-Z ^[2] /V _{SS} = 1 – PWMx value
	1	1	individual PWM (inverted)	individual PWM (inverted)	V _{DD} /V _{SS} = 1 – PWMx value

Table 15. Output transistors based on LEDOUT registers, INVRT and OUTDRV bits when $\overline{OE} = 0$ [1] ...continued

LEDOUT	INVRT	OUTDRV	Upper transistor (V _{DD} to LEDn)	Lower transistor (LEDn to V _{SS})	LEDn state
individual + group dimming/blinking	0	0	off	individual + group PWM (non-inverted)	V _{SS} /high-Z[2] = PWMx/GRPPWM values
	0	1	individual PWM (non-inverted)	individual PWM (non-inverted)	V _{SS} /V _{DD} = PWMx/GRPPWM values
	1	0	off	individual + group PWM (inverted)	high-Z[2]/V _{SS} = (1 - PWMx)/(1 - GRPPWM) values
	1	1	individual PWM (inverted)	individual PWM (inverted)	V _{DD} /V _{SS} = (1 - PWMx)/(1 - GRPPWM) values

[1] When $\overline{OE} = 1$, LED output state is controlled only by OUTNE[1:0] bits (MODE2 register).

[2] External pull-up or LED current limiting resistor connects LEDn to V_{DD}.

7.8 Individual brightness control with group dimming/blinking

A 97 kHz fixed frequency signal with programmable duty cycle (8 bits, 256 steps) is used to control individually the brightness for each LED.

On top of this signal, one of the following signals can be superimposed (this signal can be applied to the 4 LED outputs):

- A lower 190 Hz fixed frequency signal with programmable duty cycle (8 bits, 256 steps) is used to provide a global brightness control.
- A programmable frequency signal from 24 Hz to 1/10.73 s (8 bits, 256 steps) with programmable duty cycle (8 bits, 256 steps) is used to provide a global blinking control.

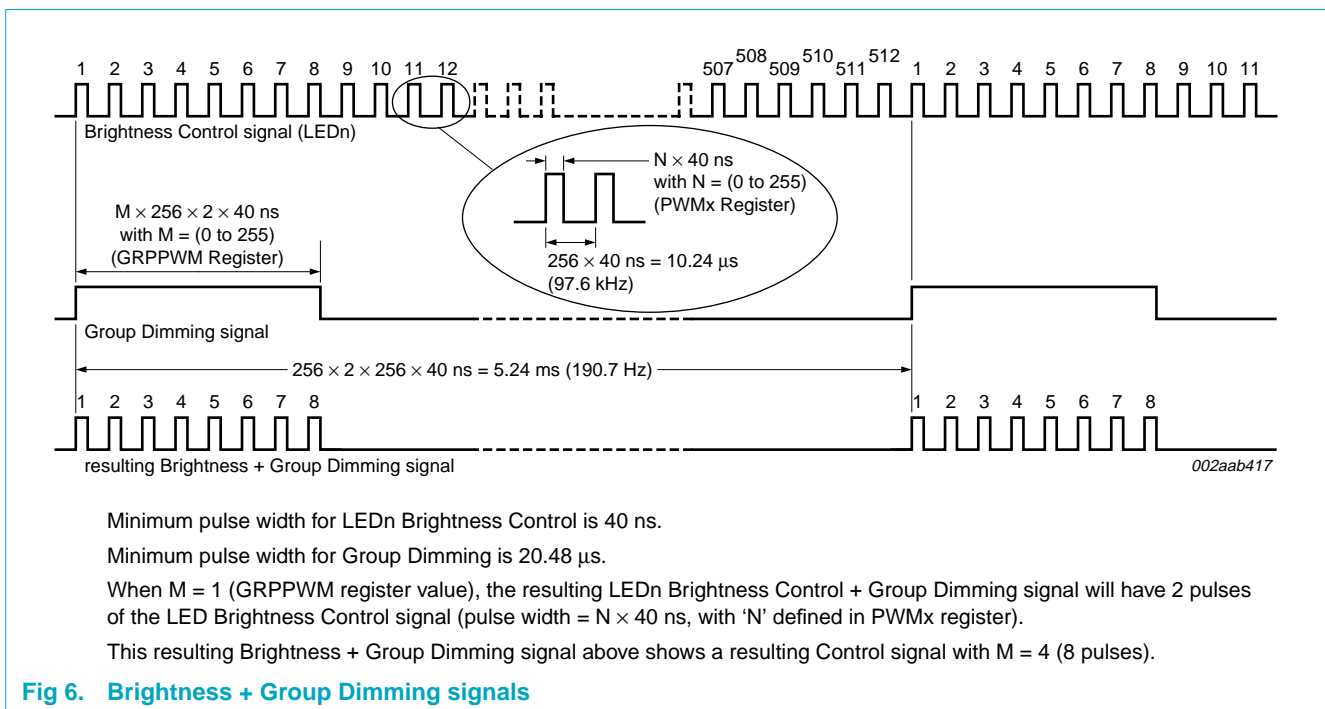


Fig 6. Brightness + Group Dimming signals

8. Characteristics of the I²C-bus

The I²C-bus is for 2-way, 2-line communication between different ICs or modules. The two lines are a serial data line (SDA) and a serial clock line (SCL). Both lines must be connected to a positive supply via a pull-up resistor when connected to the output stages of a device. Data transfer may be initiated only when the bus is not busy.

8.1 Bit transfer

One data bit is transferred during each clock pulse. The data on the SDA line must remain stable during the HIGH period of the clock pulse as changes in the data line at this time will be interpreted as control signals (see [Figure 7](#)).

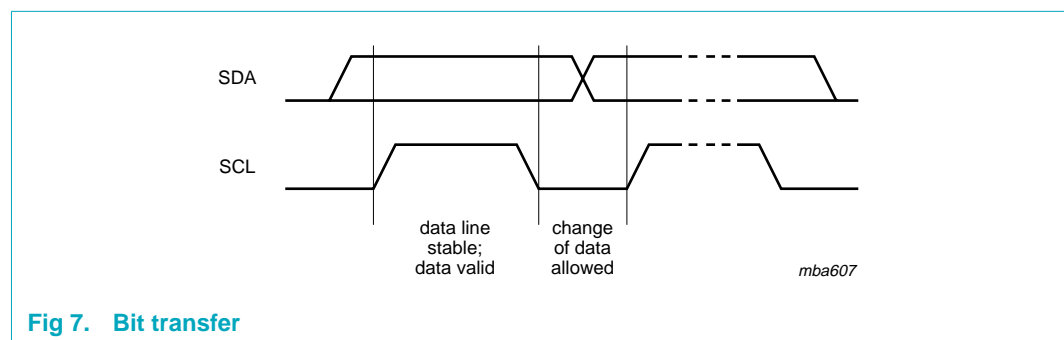


Fig 7. Bit transfer

8.1.1 START and STOP conditions

Both data and clock lines remain HIGH when the bus is not busy. A HIGH-to-LOW transition of the data line while the clock is HIGH is defined as the START condition (S). A LOW-to-HIGH transition of the data line while the clock is HIGH is defined as the STOP condition (P) (see [Figure 8](#)).

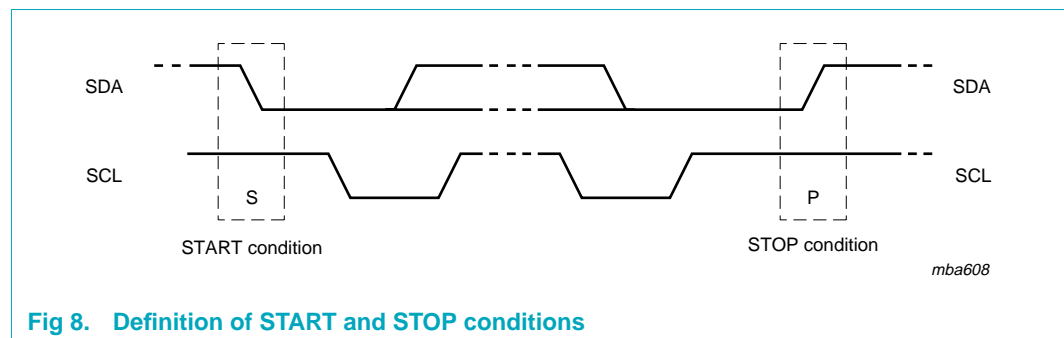


Fig 8. Definition of START and STOP conditions

8.2 System configuration

A device generating a message is a 'transmitter'; a device receiving is the 'receiver'. The device that controls the message is the 'master' and the devices which are controlled by the master are the 'slaves' (see [Figure 9](#)).

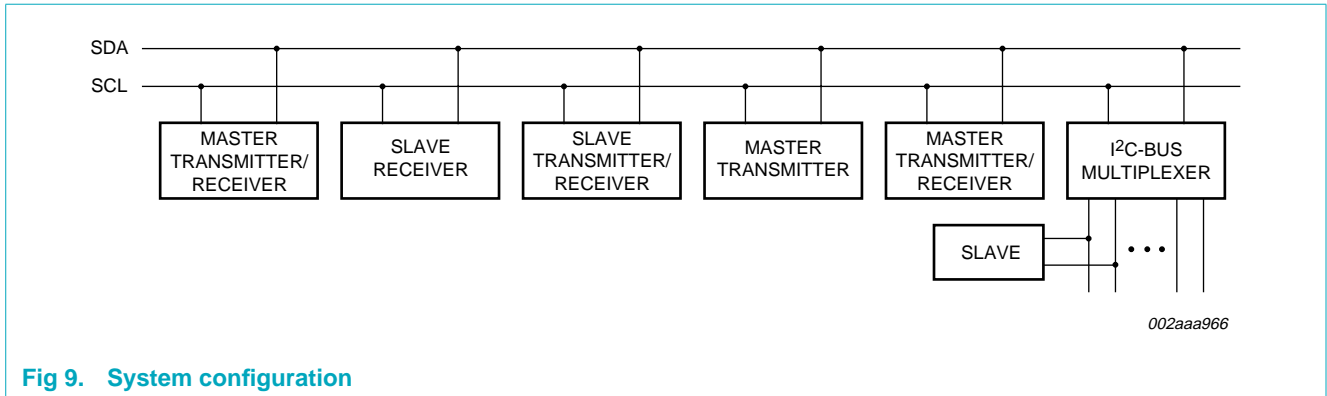


Fig 9. System configuration

8.3 Acknowledge

The number of data bytes transferred between the START and the STOP conditions from transmitter to receiver is not limited. Each byte of eight bits is followed by one acknowledge bit. The acknowledge bit is a HIGH level put on the bus by the transmitter, whereas the master generates an extra acknowledge related clock pulse.

A slave receiver which is addressed must generate an acknowledge after the reception of each byte. Also a master must generate an acknowledge after the reception of each byte that has been clocked out of the slave transmitter. The device that acknowledges has to pull down the SDA line during the acknowledge clock pulse, so that the SDA line is stable LOW during the HIGH period of the acknowledge related clock pulse; set-up time and hold time must be taken into account.

A master receiver must signal an end of data to the transmitter by not generating an acknowledge on the last byte that has been clocked out of the slave. In this event, the transmitter must leave the data line HIGH to enable the master to generate a STOP condition.

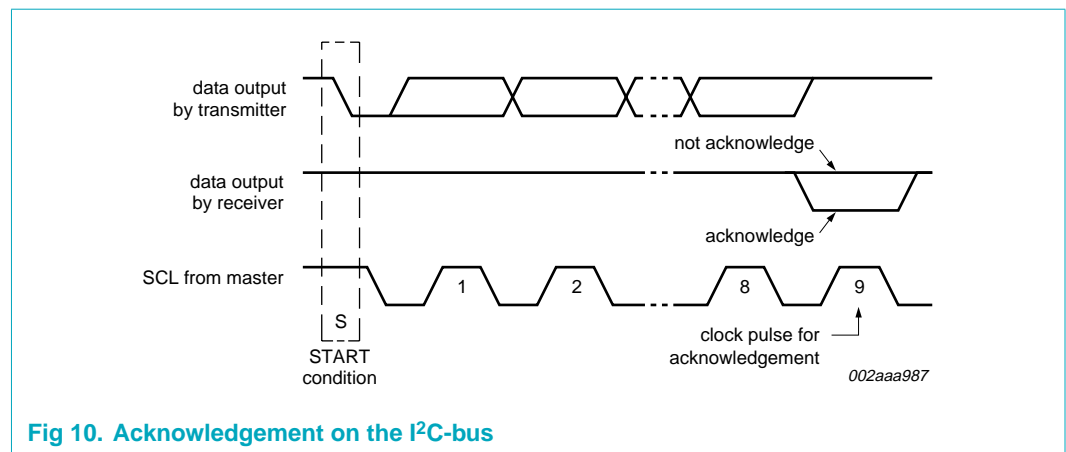
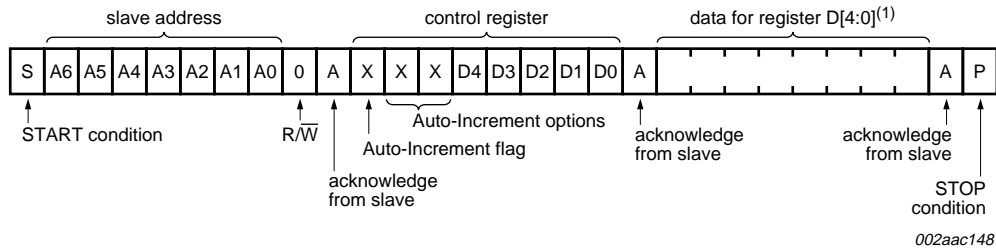


Fig 10. Acknowledgement on the I²C-bus

9. Bus transactions



(1) See Table 4 for register definition.

Fig 11. Write to a specific register

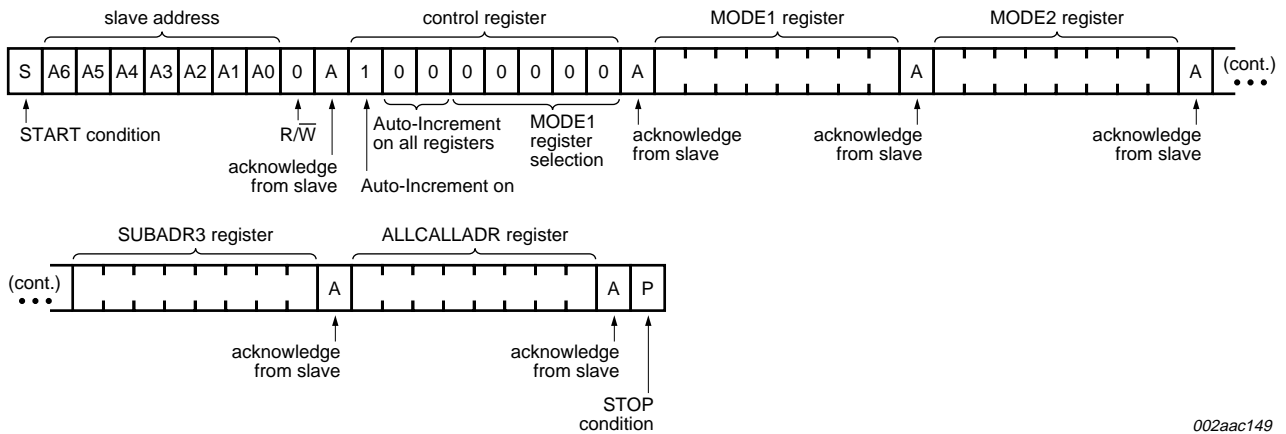


Fig 12. Write to all registers using the Auto-Increment feature

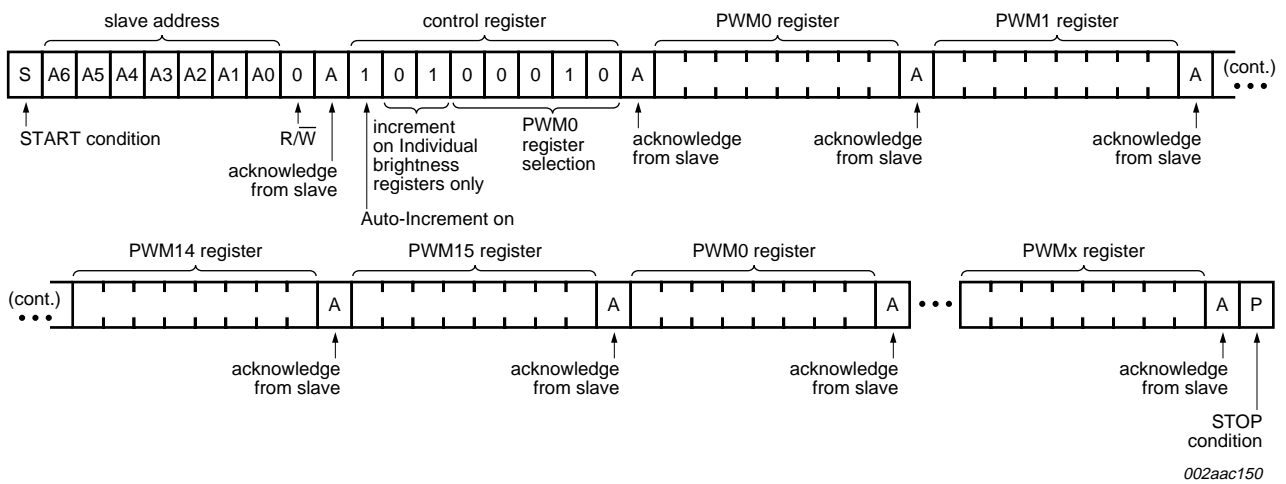


Fig 13. Multiple writes to Individual Brightness registers only using the Auto-Increment feature

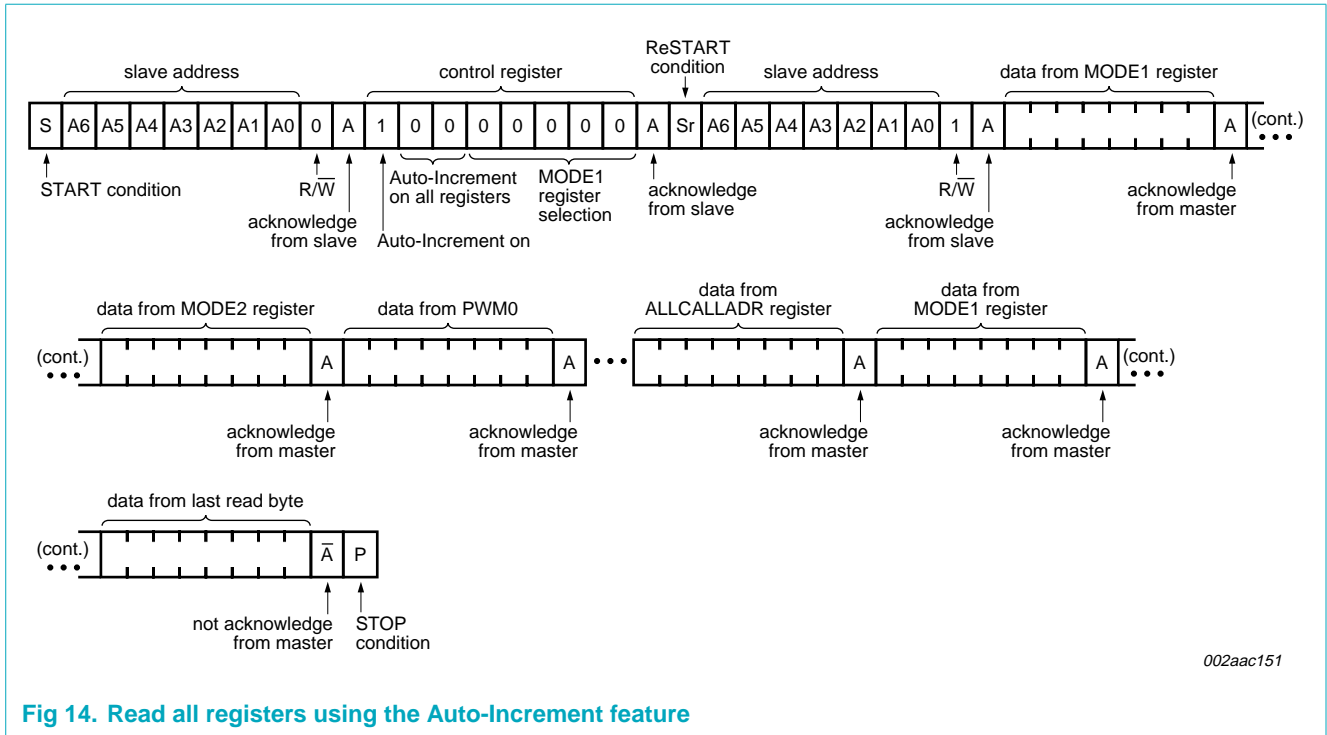
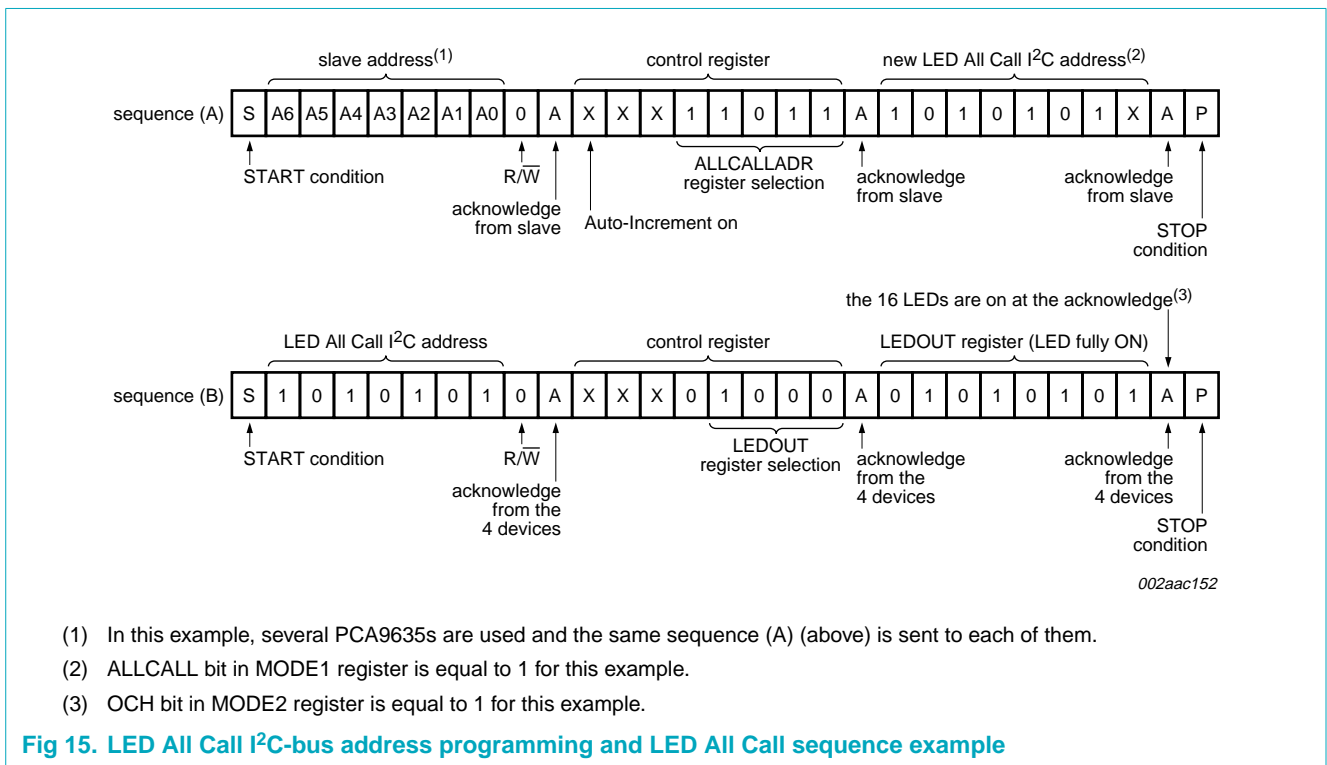


Fig 14. Read all registers using the Auto-Increment feature



- (1) In this example, several PCA9635s are used and the same sequence (A) (above) is sent to each of them.
- (2) ALLCALL bit in MODE1 register is equal to 1 for this example.
- (3) OCH bit in MODE2 register is equal to 1 for this example.

Fig 15. LED All Call I²C-bus address programming and LED All Call sequence example

10.1 LED All Call and sub register application

In this example (Figure 17), seven PCA9633s are connected to a high drive PCA9665 bus controller, so all devices are Fast-mode Plus capable. Spacing between the devices could be 1 foot to hundreds of feet, although as the bus capacitance and distance increase, the maximum communication rate will also go down. Up to 120 individually-addressed devices are allowed on the bus. This number is reduced by one for each sub call address assigned, since the total number of addresses available is 126 (128 with address reserved for LED All Call and Software Reset).

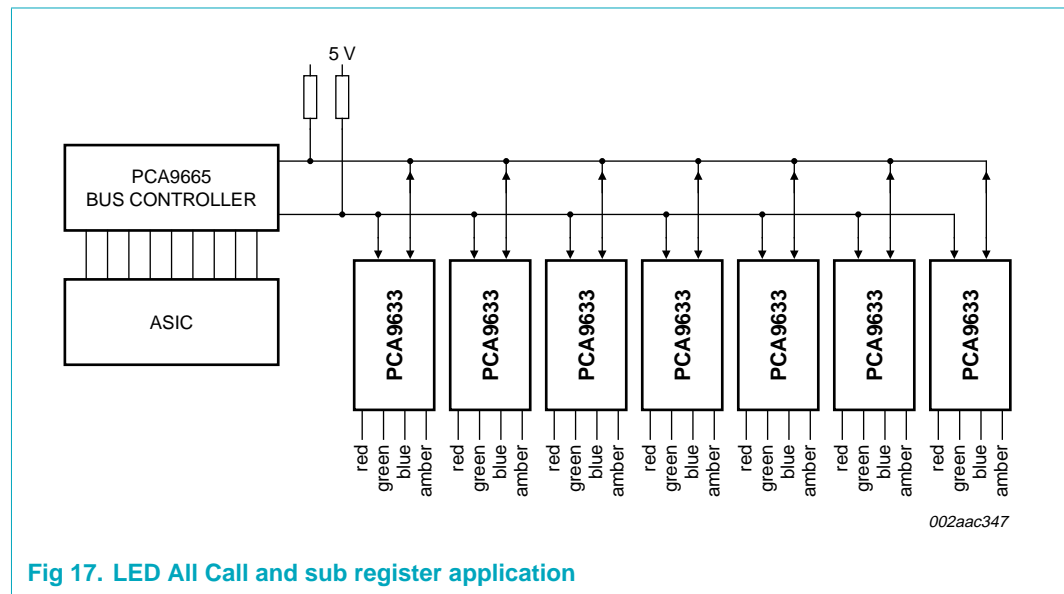


Fig 17. LED All Call and sub register application

Each PCA9633 has an individual address set by the seven hardware pins. Up to three more sub call addresses then can be programmed via the I²C-bus to allow control of groups of devices with one I²C-bus command. In this example of seven devices in a string, each device has its own individual address 1 through address 7. Additionally in LED All Call, all devices have the 126 address assigned. In Sub Call 1 alternating devices have 125, 124, and 123 addresses assigned. In Sub Call 2 there are two groups of three devices which have 122 and 121 addresses assigned. Finally in Sub Call 3, three groups of two devices have 120, 119, and 118 addresses assigned with the remaining device assigned 117 address. The device will always respond to its individual address and any sub call address it is assigned. Note that the LED All Call register can be individually changed in each device so that it can be used as a Sub Call.

Table 16. Address assignment for 7-device example

Address group	Assigned addresses						
	Device 1	Device 2	Device 3	Device 4	Device 5	Device 6	Device 7
Individual	1	2	3	4	5	6	7
LED All Call	126	126	126	126	126	126	126
Sub Call 1	125	124	123	125	124	123	125
Sub Call 2	122	122	122	-	121	121	121
Sub Call 3	120	120	119	119	118	118	117

So now these PCA9633 devices will respond to I²C-bus command to these addresses, as shown in the following examples.

10.1.1 Example 1 - individual light control

In this example, you individually control each device to program the sub registers or individually change the color or brightness of each node in the string for a wave effect.

Table 17. Individual light control addressing

Address	Device 1	Device 2	Device 3	Device 4	Device 5	Device 6	Device 7
1	X	-	-	-	-	-	-
2	-	X	-	-	-	-	-
3	-	-	X	-	-	-	-
4	-	-	-	X	-	-	-
5	-	-	-	-	X	-	-
6	-	-	-	-	-	X	-
7	-	-	-	-	-	-	X

10.1.2 Example 2 - LED All Call control

In this example, all devices will respond to the same address. With one command, all LEDs can be turned on with the same color or off at the same time, minimizing the amount of communication required and software overhead. This would be useful for gradually fading in a same color wall wash, and then gradually changing the color.

Table 18. LED All Call control addressing

Address	Device 1	Device 2	Device 3	Device 4	Device 5	Device 6	Device 7
126	X	X	X	X	X	X	X

10.1.3 Example 3 - light chasing action

In this example, every third device is assigned the same address to allow a light chasing action. It could be every other device or every fourth or fifth device, if desired. One could turn on devices 1, 4 and 7 with a single I²C-bus command, then devices 2 and 5, and then devices 3 and 6. This could be by turning address 125 on and off before the next address for a strobe-type effect, or gradually bringing one address up as the next is brought down for a color or brightness changing effect as the light chasing action continues.

Table 19. Light chasing action addressing

Address	Device 1	Device 2	Device 3	Device 4	Device 5	Device 6	Device 7
125	X	-	-	X	-	-	X
124	-	X	-	-	X	-	-
123	-	-	X	-	-	X	-

10.1.4 Example 4 - localized sub group control (2 groups of three devices)

In this example two groups of three devices have the same address. This could be used for two different wall wash colors on either end of the string with darkness in the middle.

Table 20. Localized sub group addressing

Address	Device 1	Device 2	Device 3	Device 4	Device 5	Device 6	Device 7
122	X	X	X	-	-	-	-
121	-	-	-	-	X	X	X

10.1.5 Example 5 - localized sub group control (3 groups of 2 devices)

In this example three groups of two devices have the same address, and one device has a unique address so that the groups can be controlled in any manner desired. Groups can be assigned in any fashion, and although assigning the same device (e.g., device 7) two unique individual addresses does not make sense, it could still be done.

Table 21. Localized sub group addressing

Address	Device 1	Device 2	Device 3	Device 4	Device 5	Device 6	Device 7
120	X	X	-	-	-	-	-
119	-	-	X	X	-	-	-
118	-	-	-	-	X	X	-
117	-	-	-	-	-	-	X

A good example of when this localized sub group control makes sense is where there is a 10 × 10 matrix of devices. Using the All Call, all of these devices can be turned on or off at the same time. Then localized sub groups can be assigned to:

- X shape corner to corner
- circle
- 'smiley face' inside the circle
- checkerboard pattern (alternate box addresses, like a chessboard).

Now with one I²C-bus command (or two in the case of the smiley face and checkerboard pattern), all LEDs can be turned on or off, or change color for that pattern.

The PCA9634 8-bit device and PCA9635 16-bit device can be used similarly, allowing two RGBA or four RGBA control at each node, or in the case of the PCA9634 allowing 7 LED color mixing at each node.

11. Limiting values

Table 22. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V _{DD}	supply voltage		-0.5	+6.0	V
V _{I/O}	voltage on an input/output pin		V _{SS} - 0.5	5.5	V
I _{O(LEDn)}	output current on pin LEDn		-	25	mA
I _{SS}	ground supply current		-	100	mA
P _{tot}	total power dissipation		-	400	mW
T _{stg}	storage temperature		-65	+150	°C
T _{amb}	ambient temperature	operating	-40	+85	°C

12. Static characteristics

Table 23. Static characteristics
 $V_{DD} = 2.3\text{ V to }5.5\text{ V}; V_{SS} = 0\text{ V}; T_{amb} = -40\text{ }^{\circ}\text{C to }+85\text{ }^{\circ}\text{C};$ unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Supply						
V_{DD}	supply voltage		2.3	-	5.5	V
I_{DD}	supply current	operating mode; $V_{DD} = 2.3\text{ V};$ no load; $f_{SCL} = 1\text{ MHz}$	-	2.5	10	mA
		operating mode; $V_{DD} = 3.3\text{ V};$ no load; $f_{SCL} = 1\text{ MHz}$	-	2.5	10	mA
		operating mode; $V_{DD} = 5.5\text{ V};$ no load; $f_{SCL} = 1\text{ MHz}$	-	2.5	10	mA
I_{stb}	standby current	$V_{DD} = 2.3\text{ V};$ no load; $f_{SCL} = 0\text{ Hz};$ I/O = inputs; $V_I = V_{DD}$	-	2.3	11	μA
		$V_{DD} = 3.3\text{ V};$ no load; $f_{SCL} = 0\text{ Hz};$ I/O = inputs; $V_I = V_{DD}$	-	2.9	12	μA
		$V_{DD} = 5.5\text{ V};$ no load; $f_{SCL} = 0\text{ Hz};$ I/O = inputs; $V_I = V_{DD}$	-	3.8	15.5	μA
V_{POR}	power-on reset voltage	no load; $V_I = V_{DD}$ or V_{SS}	[1] -	1.70	2.0	V
Input SCL; input/output SDA						
V_{IL}	LOW-level input voltage		-0.5	-	+0.3 V_{DD}	V
V_{IH}	HIGH-level input voltage		0.7 V_{DD}	-	5.5	V
I_{OL}	LOW-level output current	$V_{OL} = 0.4\text{ V}; V_{DD} = 2.3\text{ V}$	20	-	-	mA
		$V_{OL} = 0.4\text{ V}; V_{DD} = 5.0\text{ V}$	30	-	-	mA
I_L	leakage current	$V_I = V_{DD}$ or V_{SS}	-1	-	+1	μA
C_i	input capacitance	$V_I = V_{SS}$	-	6	10	pF
LED driver outputs						
I_{OL}	LOW-level output current	$V_{OL} = 0.5\text{ V}; V_{DD} = 2.3\text{ V}$	[2] 12	-	-	mA
		$V_{OL} = 0.5\text{ V}; V_{DD} = 3.0\text{ V}$	[2] 17	-	-	mA
		$V_{OL} = 0.5\text{ V}; V_{DD} = 4.5\text{ V}$	[2] 25	-	-	mA
$I_{OL(tot)}$	total LOW-level output current	$V_{OL} = 0.5\text{ V}; V_{DD} = 4.5\text{ V}$	[2] -	-	400	mA
I_{OH}	HIGH-level output current	open-drain; $V_{OH} = V_{DD}$	-50	-	+50	μA
V_{OH}	HIGH-level output voltage	$I_{OH} = -10\text{ mA}; V_{DD} = 2.3\text{ V}$	1.6	-	-	V
		$I_{OH} = -10\text{ mA}; V_{DD} = 3.0\text{ V}$	2.3	-	-	V
		$I_{OH} = -10\text{ mA}; V_{DD} = 4.5\text{ V}$	4.0	-	-	V
C_o	output capacitance		-	2.5	5	pF
O_E input						
V_{IL}	LOW-level input voltage		-0.5	-	+0.8	V
V_{IH}	HIGH-level input voltage		2	-	5.5	V
I_{LI}	input leakage current		-1	-	+1	μA
C_i	input capacitance		-	3.7	5	pF

Table 23. Static characteristics ...continued

$V_{DD} = 2.3\text{ V to }5.5\text{ V}$; $V_{SS} = 0\text{ V}$; $T_{amb} = -40\text{ °C to }+85\text{ °C}$; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Address inputs						
V_{IL}	LOW-level input voltage		-0.5	-	+0.3 V_{DD}	V
V_{IH}	HIGH-level input voltage		0.7 V_{DD}	-	5.5	V
I_{LI}	input leakage current		-1	-	+1	μA
C_i	input capacitance		-	3.7	5	pF

[1] V_{DD} must be lowered to 0.2 V in order to reset part.

[2] Each bit must be limited to a maximum of 25 mA and the total package limited to 400 mA due to internal busing limits.

13. Dynamic characteristics

Table 24. Dynamic characteristics

Symbol	Parameter	Conditions	Standard-mode I ² C-bus		Fast-mode I ² C-bus		Fast-mode Plus I ² C-bus		Unit
			Min	Max	Min	Max	Min	Max	
f_{SCL}	SCL clock frequency	[1]	0	100	0	400	0	1000	kHz
t_{BUF}	bus free time between a STOP and START condition		4.7	-	1.3	-	0.5	-	μs
$t_{HD;STA}$	hold time (repeated) START condition		4.0	-	0.6	-	0.26	-	μs
$t_{SU;STA}$	set-up time for a repeated START condition		4.7	-	0.6	-	0.26	-	μs
$t_{SU;STO}$	set-up time for STOP condition		4.0	-	0.6	-	0.26	-	μs
$t_{HD;DAT}$	data hold time		0	-	0	-	0	-	ns
$t_{VD;ACK}$	data valid acknowledge time	[2]	0.3	3.45	0.1	0.9	0.05	0.45	μs
$t_{VD;DAT}$	data valid time	[3]	0.3	3.45	0.1	0.9	0.05	0.45	μs
$t_{SU;DAT}$	data set-up time		250	-	100	-	50	-	ns
t_{LOW}	LOW period of the SCL clock		4.7	-	1.3	-	0.5	-	μs
t_{HIGH}	HIGH period of the SCL clock		4.0	-	0.6	-	0.26	-	μs
t_f	fall time of both SDA and SCL signals	[5][6]	-	300	$20 + 0.1C_b$ [4]	300	-	120	ns
t_r	rise time of both SDA and SCL signals		-	1000	$20 + 0.1C_b$ [4]	300	-	120	ns
t_{SP}	pulse width of spikes that must be suppressed by the input filter	[7]	-	50	-	50	-	50	ns

[1] Minimum SCL clock frequency is limited by the bus time-out feature, which resets the serial bus interface if either SDA or SCL is held LOW for a minimum of 25 ms. Disable bus time-out feature for DC operation.

[2] $t_{VD;ACK}$ = time for Acknowledgement signal from SCL LOW to SDA (out) LOW.

[3] $t_{VD;DAT}$ = minimum time for SDA data out to be valid following SCL LOW.

[4] C_b = total capacitance of one bus line in pF.

[5] A master device must internally provide a hold time of at least 300 ns for the SDA signal (refer to the V_{IL} of the SCL signal) in order to bridge the undefined region of SCL's falling edge.

- [6] The maximum t_r for the SDA and SCL bus lines is specified at 300 ns. The maximum fall time (t_f) for the SDA output stage is specified at 250 ns. This allows series protection resistors to be connected between the SDA and the SCL pins and the SDA/SCL bus lines without exceeding the maximum specified t_r .
- [7] Input filters on the SDA and SCL inputs suppress noise spikes less than 50 ns.

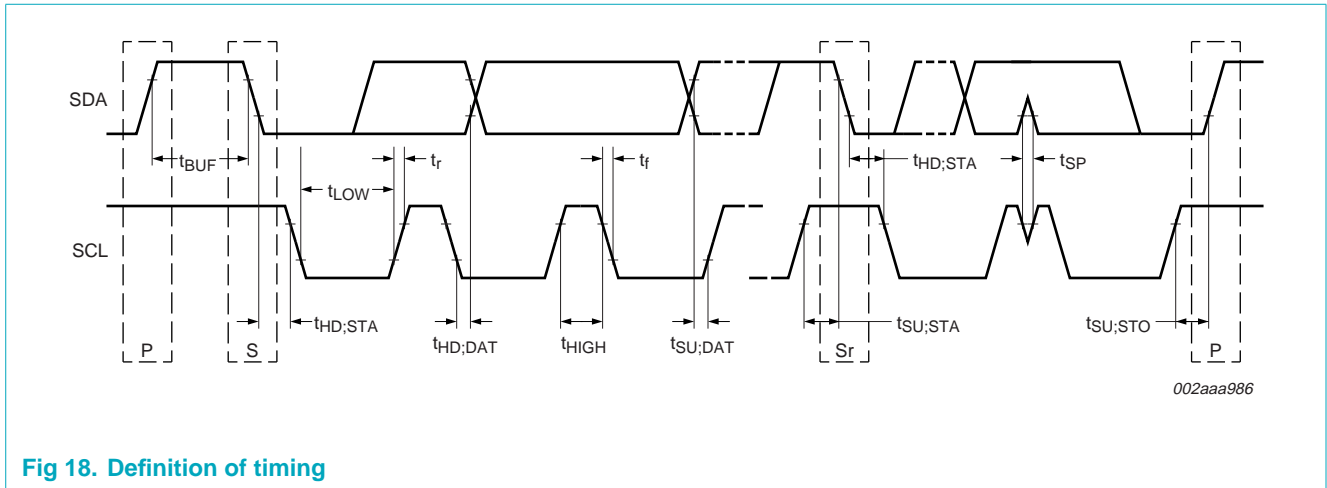


Fig 18. Definition of timing

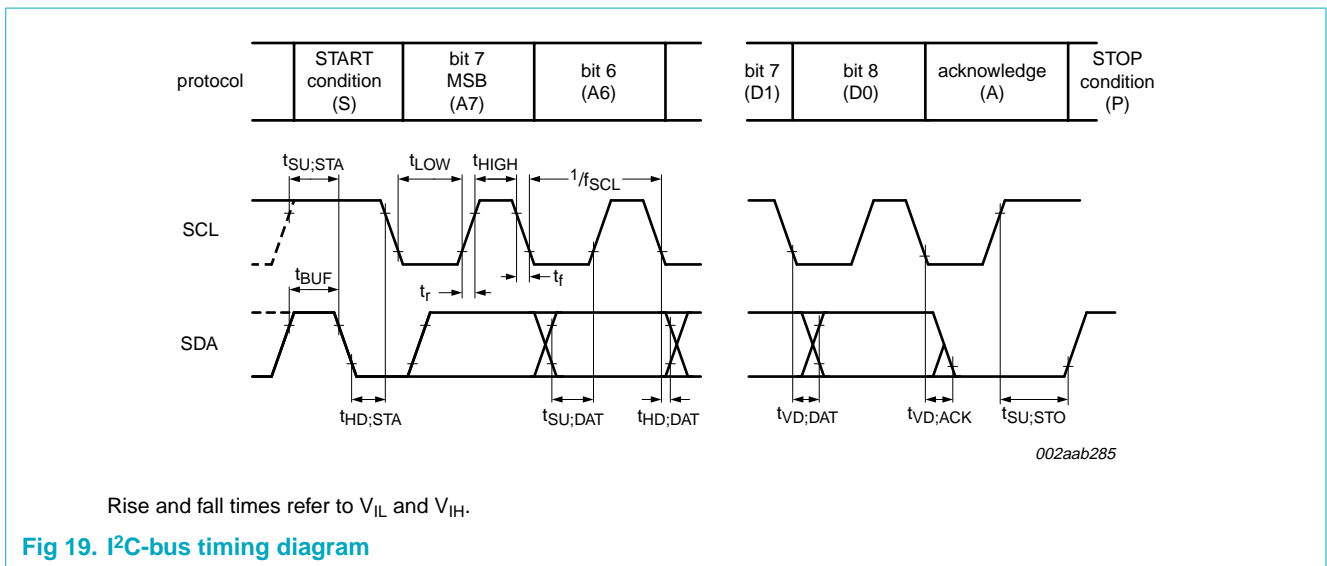
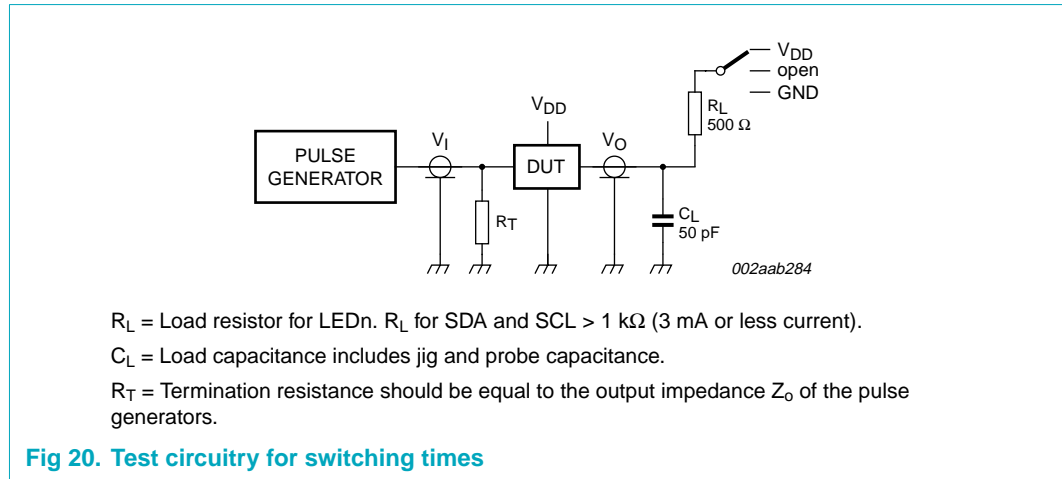


Fig 19. I²C-bus timing diagram

14. Test information



15. Package outline

TSSOP28: plastic thin shrink small outline package; 28 leads; body width 4.4 mm

SOT361-1

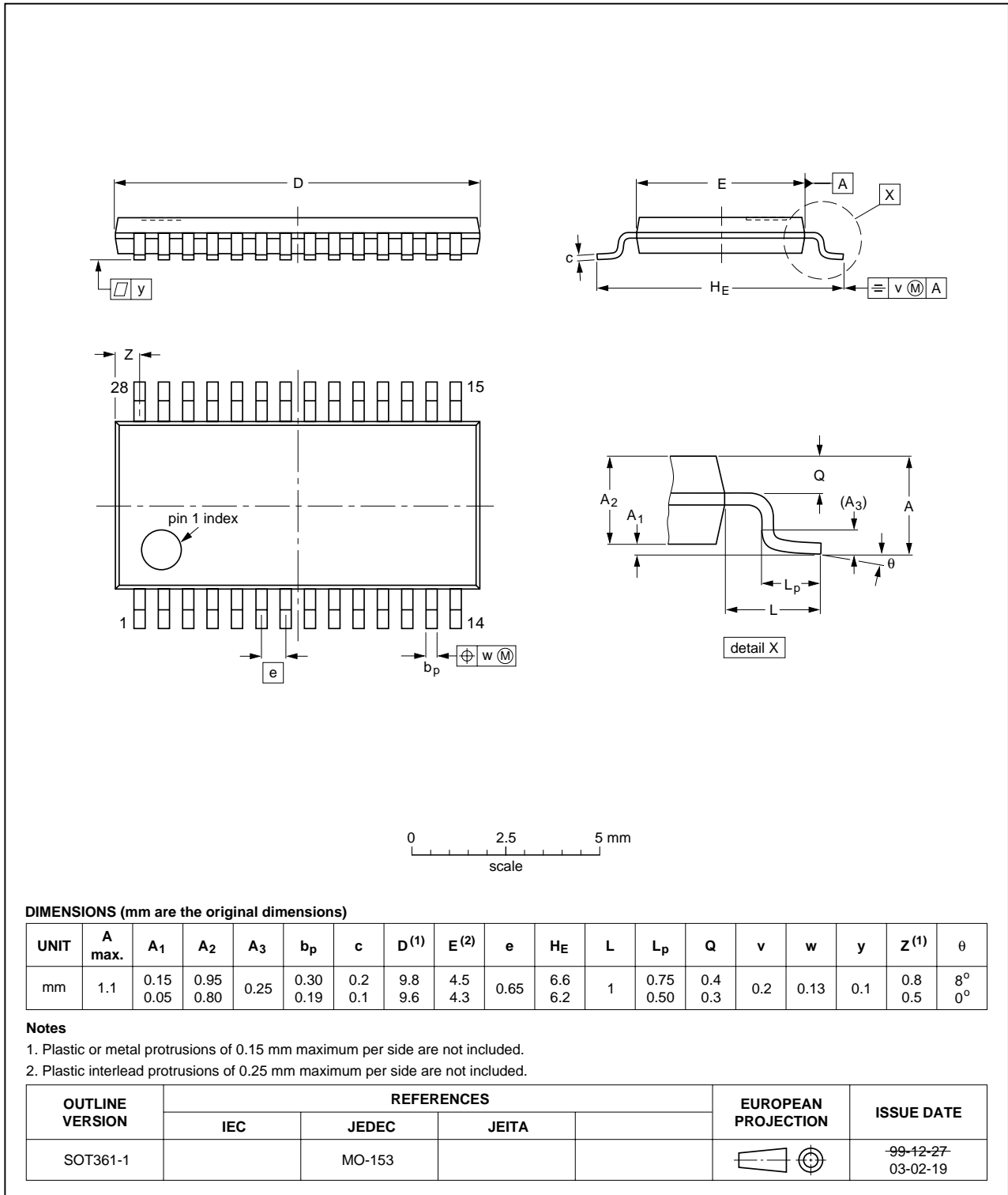


Fig 21. Package outline SOT361-1 (TSSOP28)

16. Handling information

Inputs and outputs are protected against electrostatic discharge in normal handling. However, to be completely safe you must take normal precautions appropriate to handling integrated circuits.

17. Soldering

17.1 Introduction to soldering surface mount packages

There is no soldering method that is ideal for all surface mount IC packages. Wave soldering can still be used for certain surface mount ICs, but it is not suitable for fine pitch SMDs. In these situations reflow soldering is recommended.

17.2 Reflow soldering

Reflow soldering requires solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the printed-circuit board by screen printing, stencilling or pressure-syringe dispensing before package placement. Driven by legislation and environmental forces the worldwide use of lead-free solder pastes is increasing.

Several methods exist for reflowing; for example, convection or convection/infrared heating in a conveyor type oven. Throughput times (preheating, soldering and cooling) vary between 100 seconds and 200 seconds depending on heating method.

Typical reflow temperatures range from 215 °C to 260 °C depending on solder paste material. The peak top-surface temperature of the packages should be kept below:

Table 25. SnPb eutectic process - package peak reflow temperatures (from J-STD-020C July 2004)

Package thickness	Volume mm ³ < 350	Volume mm ³ ≥ 350
< 2.5 mm	240 °C + 0/-5 °C	225 °C + 0/-5 °C
≥ 2.5 mm	225 °C + 0/-5 °C	225 °C + 0/-5 °C

Table 26. Pb-free process - package peak reflow temperatures (from J-STD-020C July 2004)

Package thickness	Volume mm ³ < 350	Volume mm ³ 350 to 2000	Volume mm ³ > 2000
< 1.6 mm	260 °C + 0 °C	260 °C + 0 °C	260 °C + 0 °C
1.6 mm to 2.5 mm	260 °C + 0 °C	250 °C + 0 °C	245 °C + 0 °C
≥ 2.5 mm	250 °C + 0 °C	245 °C + 0 °C	245 °C + 0 °C

Moisture sensitivity precautions, as indicated on packing, must be respected at all times.

17.3 Wave soldering

Conventional single wave soldering is not recommended for surface mount devices (SMDs) or printed-circuit boards with a high component density, as solder bridging and non-wetting can present major problems.

To overcome these problems the double-wave soldering method was specifically developed.

If wave soldering is used the following conditions must be observed for optimal results:

- Use a double-wave soldering method comprising a turbulent wave with high upward pressure followed by a smooth laminar wave.
- For packages with leads on two sides and a pitch (e):
 - larger than or equal to 1.27 mm, the footprint longitudinal axis is **preferred** to be parallel to the transport direction of the printed-circuit board;
 - smaller than 1.27 mm, the footprint longitudinal axis **must** be parallel to the transport direction of the printed-circuit board.

The footprint must incorporate solder thieves at the downstream end.

- For packages with leads on four sides, the footprint must be placed at a 45° angle to the transport direction of the printed-circuit board. The footprint must incorporate solder thieves downstream and at the side corners.

During placement and before soldering, the package must be fixed with a droplet of adhesive. The adhesive can be applied by screen printing, pin transfer or syringe dispensing. The package can be soldered after the adhesive is cured.

Typical dwell time of the leads in the wave ranges from 3 seconds to 4 seconds at 250 °C or 265 °C, depending on solder material applied, SnPb or Pb-free respectively.

A mildly-activated flux will eliminate the need for removal of corrosive residues in most applications.

17.4 Manual soldering

Fix the component by first soldering two diagonally-opposite end leads. Use a low voltage (24 V or less) soldering iron applied to the flat part of the lead. Contact time must be limited to 10 seconds at up to 300 °C.

When using a dedicated tool, all other leads can be soldered in one operation within 2 seconds to 5 seconds between 270 °C and 320 °C.

17.5 Package related soldering information

Table 27. Suitability of surface mount IC packages for wave and reflow soldering methods

Package ^[1]	Soldering method	
	Wave	Reflow ^[2]
BGA, HTSSON..T ^[3] , LBGA, LFBGA, SQFP, SSOP..T ^[3] , TFBGA, VFBGA, XSON	not suitable	suitable
DHVQFN, HBCC, HBGA, HLQFP, HSO, HSOP, HSQFP, HSSON, HTQFP, HTSSOP, HVQFN, HVSON, SMS	not suitable ^[4]	suitable
PLCC ^[5] , SO, SOJ	suitable	suitable
LQFP, QFP, TQFP	not recommended ^{[5][6]}	suitable
SSOP, TSSOP, VSO, VSSOP	not recommended ^[7]	suitable
CWQCCN..L ^[8] , PMFP ^[9] , WQCCN..L ^[8]	not suitable	not suitable

- [1] For more detailed information on the BGA packages refer to the *(LF)BGA Application Note (AN01026)*; order a copy from your Philips Semiconductors sales office.
- [2] All surface mount (SMD) packages are moisture sensitive. Depending upon the moisture content, the maximum temperature (with respect to time) and body size of the package, there is a risk that internal or external package cracks may occur due to vaporization of the moisture in them (the so called popcorn effect). For details, refer to the Drypack information in the *Data Handbook IC26; Integrated Circuit Packages; Section: Packing Methods*.
- [3] These transparent plastic packages are extremely sensitive to reflow soldering conditions and must on no account be processed through more than one soldering cycle or subjected to infrared reflow soldering with peak temperature exceeding $217\text{ °C} \pm 10\text{ °C}$ measured in the atmosphere of the reflow oven. The package body peak temperature must be kept as low as possible.
- [4] These packages are not suitable for wave soldering. On versions with the heatsink on the bottom side, the solder cannot penetrate between the printed-circuit board and the heatsink. On versions with the heatsink on the top side, the solder might be deposited on the heatsink surface.
- [5] If wave soldering is considered, then the package must be placed at a 45° angle to the solder wave direction. The package footprint must incorporate solder thieves downstream and at the side corners.
- [6] Wave soldering is suitable for LQFP, QFP and TQFP packages with a pitch (e) larger than 0.8 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.65 mm.
- [7] Wave soldering is suitable for SSOP, TSSOP, VSO and VSSOP packages with a pitch (e) equal to or larger than 0.65 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.5 mm.
- [8] Image sensor packages in principle should not be soldered. They are mounted in sockets or delivered pre-mounted on flex foil. However, the image sensor package can be mounted by the client on a flex foil by using a hot bar soldering process. The appropriate soldering profile can be provided on request.
- [9] Hot bar soldering or manual soldering is suitable for PMFP packages.

18. Abbreviations

Table 28. Abbreviations

Acronym	Description
CDM	Charged Device Model
DUT	Device Under Test
ESD	ElectroStatic Discharge
HBM	Human Body Model
I ² C-bus	Inter-Integrated Circuit bus
LED	Light Emitting Diode
LSB	Least Significant Bit
MM	Machine Model
PCB	Printed-Circuit Board
PWM	Pulse Width Modulation
RGB	Red/Green/Blue
RGBA	Red/Green/Blue/Amber
SMBus	System Management Bus

19. Revision history

Table 29. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
PCA9635_2	20060807	Objective data sheet	-	PCA9635_1
Modifications:		<ul style="list-style-type: none"> • data sheet descriptive title changed from “16-bit I²C-bus LED driver” to “16-bit Fm+ I²C-bus LED driver” • Section 1 “General description”: added new 3rd paragraph and new 6th paragraph • Section 2 “Features”: <ul style="list-style-type: none"> – 2nd bullet: changed from “1 MHz Fast mode compatible I²C-bus interface ...” to “1 MHz Fast-mode Plus I²C-bus interface ...” – added (new) 11th bullet • binary numbers: added separator space following 4th MSB digit • hex numbers: changed format from, e.g., “0xXX” to “XXh” • all “Caution” texts changed to “Remark” • Section 7.1.3 “LED Sub Call I²C-bus addresses”, 2nd bullet, 3rd sub-bullet: changed “SUBADR2 register:” to “SUBADR3 register:” • added new Section 7.1.4 “Software Reset I²C-bus address” • Section 7.3.8 “ALLCALLADR, LED All Call I²C-bus address”: added last sentence to paragraph following Table 12 • added new Section 7.6 “Software Reset” • added new Section 10.1 “LED All Call and sub register application” • Table 23 “Static characteristics”: <ul style="list-style-type: none"> – added Table note 2 and references to it at I_{OL} and I_{OL(tot)} under sub-section “LED driver outputs” • Section 17 “Soldering” updated 		
PCA9635_1	20060419	Objective data sheet	-	-

20. Legal information

20.1 Data sheet status

Document status ^{[1][2]}	Product status ^[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

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