PCA9517

Level translating I²C-bus repeater

Rev. 02 — 15 June 2006 Product data sheet

1. General description

The PCA9517 is a CMOS integrated circuit that provides level shifting between low voltage (down to 0.9 V) and higher voltage (2.7 V to 5.5 V) I²C-bus or SMBus applications. While retaining all the operating modes and features of the I²C-bus system during the level shifts, it also permits extension of the I²C-bus by providing bidirectional buffering for both the data (SDA) and the clock (SCL) lines, thus enabling two buses of 400 pF. Using the PCA9517 enables the system designer to isolate two halves of a bus for both voltage and capacitance. The SDA and SCL pins are over voltage tolerant and are high-impedance when the PCA9517 is unpowered.

The 2.7 V to 5.5 V bus B side drivers behave much like the drivers on the PCA9515A device, while the adjustable voltage bus A side drivers drive more current and eliminate the static offset voltage. This results in a LOW on the B side translating into a nearly 0 V LOW on the A side which accommodates smaller voltage swings of lower voltage logic.

The static offset design of the B side PCA9517 I/O drivers prevent them from being connected to another device that has rise time accelerator including the PCA9510, PCA9511, PCA9512, PCA9513, PCA9514, PCA9515A, PCA9516A, PCA9517 (B side), or PCA9518. The A side of two or more PCA9517s can be connected together, however, to allow a star topography with the A side on the common bus, and the A side can be connected directly to any other buffer with static or dynamic offset voltage. Multiple PCA9517s can be connected in series, A side to B side, with no build-up in offset voltage with only time of flight delays to consider.

The PCA9517 drivers are not enabled unless V_{CCA} is above 0.8 V and V_{CC} is above 2.5 V. The EN pin can also be used to turn the drivers on and off under system control. Caution should be observed to only change the state of the enable pin when the bus is idle.

The output pull-down on the B side internal buffer LOW is set for approximately 0.5 V, while the input threshold of the internal buffer is set about 70 mV lower (0.43 V). When the B side I/O is driven LOW internally, the LOW is not recognized as a LOW by the input. This prevents a lock-up condition from occurring. The output pull-down on the A side drives a hard LOW and the input level is set at $0.3V_{CCA}$ to accommodate the need for a lower LOW level in systems where the low voltage side supply voltage is as low as 0.9 V.

2. Features

- 2 channel, bidirectional buffer isolates capacitance and allows 400 pF on either side of the device
- Voltage level translation from 0.9 V to 5.5 V and from 2.7 V to 5.5 V
- Footprint and functional replacement for PCA9515/15A
- I²C-bus and SMBus compatible

PHILIPS

- Active HIGH repeater enable input
- Open-drain input/outputs
- Lock-up free operation
- Supports arbitration and clock stretching across the repeater
- Accommodates Standard mode and Fast mode I²C-bus devices and multiple masters
- Powered-off high-impedance I²C-bus pins
- A side operating supply voltage range of 0.9 V to 5.5 V
- B side operating supply voltage range of 2.7 V to 5.5 V
- 5 V tolerant I²C-bus and enable pins
- 0 Hz to 400 kHz clock frequency (the maximum system operating frequency may be less than 400 kHz because of the delays added by the repeater).
- ESD protection exceeds 2000 V HBM per JESD22-A114, 200 V MM per JESD22-A115, and 1000 V CDM per JESD22-C101
- Latch-up testing is done to JEDEC Standard JESD78 which exceeds 100 mA
- Packages offered: SO8 and TSSOP8

3. Ordering information

Table 1: Ordering information

T_{amb} = −40 °C to +85 °C

Type number	Topside mark	Package		
		Name	Description	Version
PCA9517D	PCA9517	SO8	plastic small outline package; 8 leads; body width 3.9 mm	SOT96-1
PCA9517DP	9517	TSSOP8 [1]	plastic thin shrink small outline package; 8 leads; body width 3 mm	SOT505-1

[1] Also known as MSOP8

4. Functional diagram

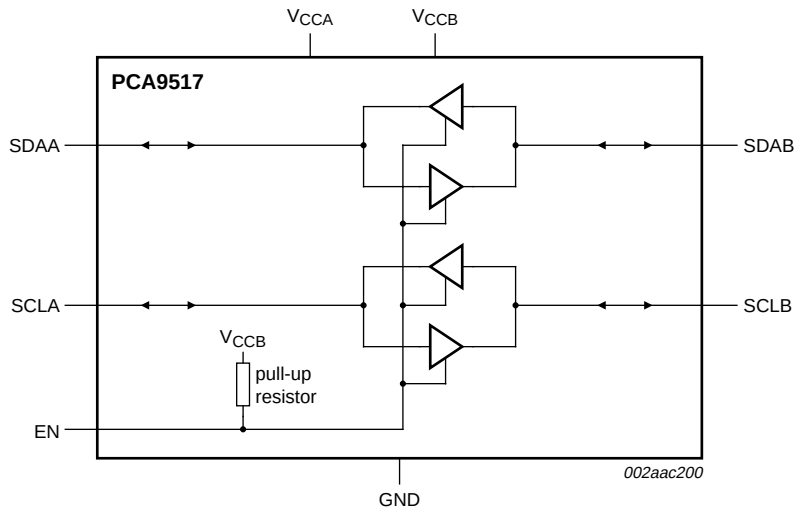


Fig 1. Functional diagram of PCA9517

5. Pinning information

5.1 Pinning

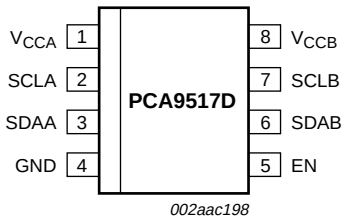


Fig 2. Pin configuration for SO8

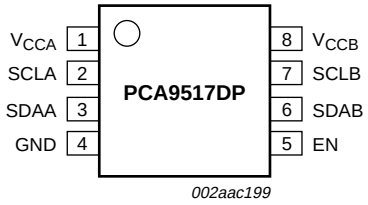


Fig 3. Pin configuration for TSSOP8

5.2 Pin description

Table 2: Pin description

Symbol	Pin	Description
V_{CCA}	1	A side supply voltage (0.9 V to 5.5 V)
SCLA	2	serial clock A side bus
SDAA	3	serial data A side bus
GND	4	supply ground (0 V)
EN	5	active HIGH repeater enable input
SDAB	6	serial data B side bus
SCLB	7	serial clock B side bus
V_{CCB}	8	B side supply voltage (2.7 V to 5.5 V)

6. Functional description

Refer to Figure 1 “Functional diagram of PCA9517”.

The PCA9517 enables I²C-bus or SMBus translation down to V_{CCA} as low as 0.9 V without degradation of system performance. The PCA9517 contains two bidirectional open-drain buffers specifically designed to support up-translation/down-translation between the low voltage (as low as 0.9 V) and a 3.3 V or 5 V I²C-bus or SMBus. All inputs and I/Os are overvoltage tolerant to 5.5 V even when the device is unpowered (V_{CCB} and/or V_{CCA} = 0 V). The PCA9517 includes a power-up circuit that keeps the output drivers turned off until V_{CCB} is above 2.5 V and the V_{CCA} is above 0.8 V. V_{CCB} and V_{CCA} can be applied in any sequence at power-up. After power-up and with the enable (EN) HIGH, a LOW level on the A side (below $0.3V_{CCA}$) turns the corresponding B side driver (either SDA or SCL) on and drives the B side down to about 0.5 V. When the A side rises above $0.3V_{CCA}$ the B side pull-down driver is turned off and the external pull-up resistor pulls the pin HIGH. When the B side falls first and goes below $0.3V_{CCB}$ the A side driver is turned on and the A side pulls down to 0 V. The B side pull-down is not enabled unless the B side voltage goes below 0.4 V. If the B side low voltage does not go below 0.5 V, the A side driver will turn off when the B side voltage is above $0.7V_{CCB}$. If the B side low voltage goes below 0.4 V, the B side pull-down driver is enabled and the B side will only be able to rise to 0.5 V until the A side rises above $0.3V_{CCA}$, then the B side will continue

to rise being pulled up by the external pull-up resistor. The V_{CCA} is only used to provide the $0.3V_{CCA}$ reference to the A side input comparators and for the power good detect circuit. The PCA9517 logic and all I/Os are powered by the V_{CCB} pin.

6.1 Enable

The EN pin is active HIGH with an internal pull-up to V_{CCB} and allows the user to select when the repeater is active. This can be used to isolate a badly behaved slave on power-up until after the system power-up reset. It should never change state during an I²C-bus operation because disabling during a bus operation will hang the bus and enabling part way through a bus cycle could confuse the I²C-bus parts being enabled.

The enable pin should only change state when the global bus and the repeater port are in an idle state to prevent system failures.

6.2 I²C-bus systems

As with the standard I²C-bus system, pull-up resistors are required to provide the logic HIGH levels on the buffered bus (standard open-collector configuration of the I²C-bus). The size of these pull-up resistors depends on the system, but each side of the repeater must have a pull-up resistor. This part designed to work with Standard mode and Fast mode I²C-bus devices in addition to SMBus devices. Standard mode I²C-bus devices only specify 3 mA output drive; this limits the termination current to 3 mA in a generic I²C-bus system where Standard mode devices and multiple masters are possible. Under certain conditions higher termination currents can be used.

Please see Application Note *AN255, I²C/SMBus Repeaters, Hubs and Expanders* for additional information on sizing resistors and precautions when using more than one PCA9517 in a system or using the PCA9517 in conjunction with other bus buffers.

7. Application design-in information

A typical application is shown in Figure 4. In this example, the system master is running on a 3.3 V I²C-bus while the slave is connected to a 1.2 V bus. Both buses run at 400 kHz. Master devices can be placed on either bus.

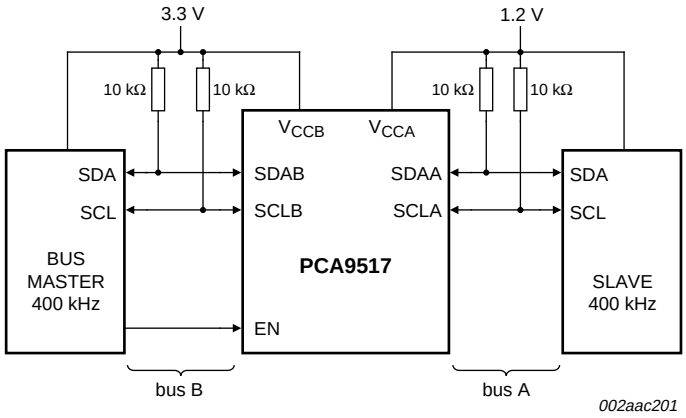


Fig 4. Typical application

The PCA9517 is 5 V tolerant, so it does not require any additional circuitry to translate between 0.9 V to 5.5 V bus voltages and 2.7 V to 5.5 V bus voltages.

When the A side of the PCA9517 is pulled LOW by a driver on the I²C-bus, a comparator detects the falling edge when it goes below $0.3V_{CCA}$ and causes the internal driver on the B side to turn on, causing the B side to pull down to about 0.5 V. When the B side of the PCA9517 falls, first a CMOS hysteresis type input detects the falling edge and causes the internal driver on the A side to turn on and pull the A side pin down to ground. In order to illustrate what would be seen in a typical application, refer to Figure 7 and Figure 8. If the bus master in Figure 4 were to write to the slave through the PCA9517, waveforms shown in Figure 7 would be observed on the A bus. This looks like a normal I²C-bus transmission except that the HIGH level may be as low as 0.9 V, and the turn on and turn off of the acknowledge signals are slightly delayed.

On the B bus side of the PCA9517, the clock and data lines would have a positive offset from ground equal to the V_{OL} of the PCA9517. After the 8th clock pulse, the data line will be pulled to the V_{OL} of the slave device which is very close to ground in this example. At the end of the acknowledge, the level rises only to the LOW level set by the driver in the PCA9517 for a short delay while the A bus side rises above $0.3V_{CCA}$ then it continues HIGH. It is important to note that any arbitration or clock stretching events require that the LOW level on the B bus side at the input of the PCA9517 (V_{IL}) be at or below 0.4 V to be recognized by the PCA9517 and then transmitted to the A bus side.

Multiple PCA9517 A sides can be connected in a star configuration (Figure 5), allowing all nodes to communicate with each other.

Multiple PCA9517s can be connected in series (Figure 6) as long as the A side is connected to the B side. I²C-bus slave devices can be connected to any of the bus segments. The number of devices that can be connected in series is limited by repeater delay/time-of-flight considerations on the maximum bus speed requirements.

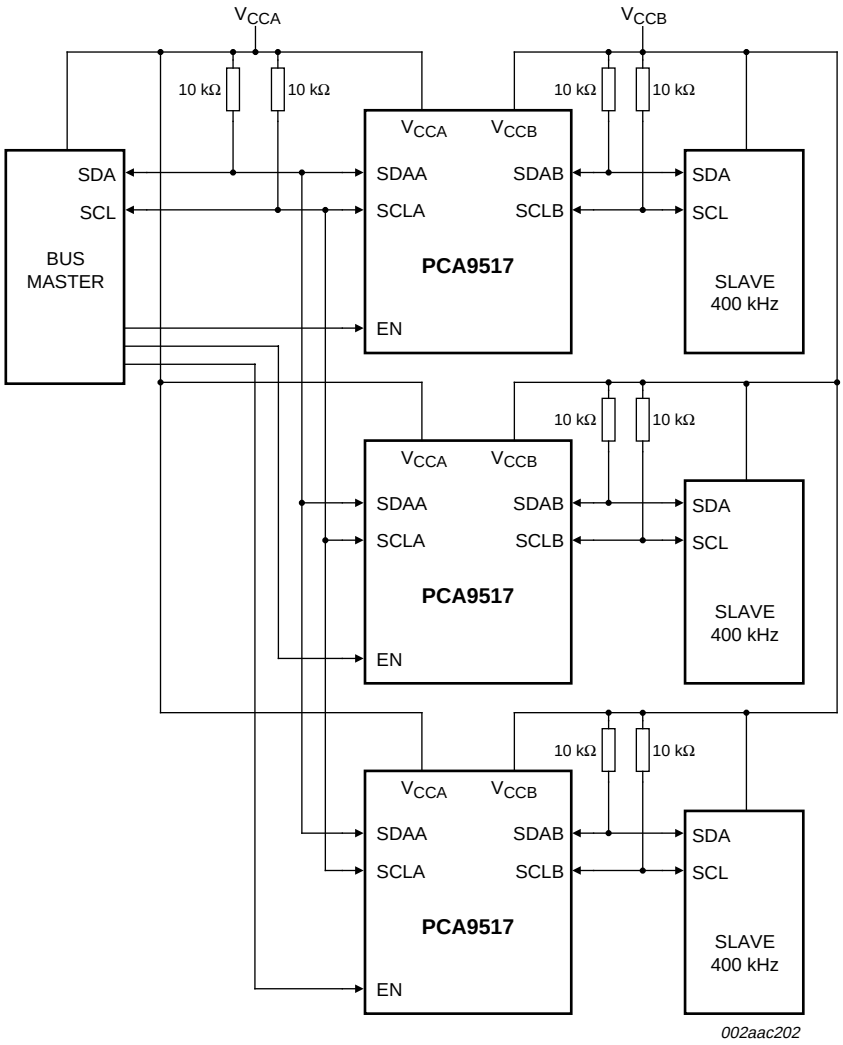


Fig 5. Typical star application

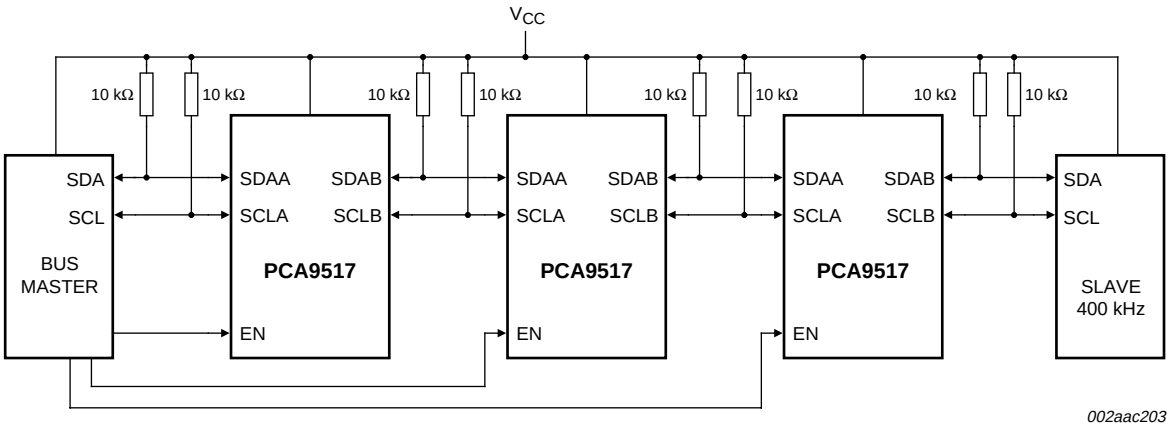


Fig 6. Typical series application

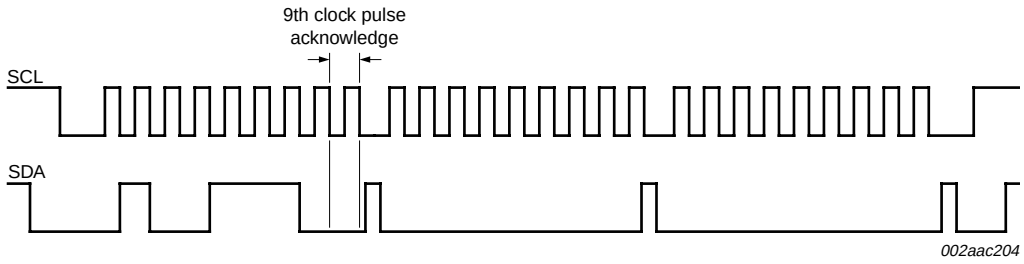


Fig 7. Bus A (0.9 V to 5.5 V bus) waveform

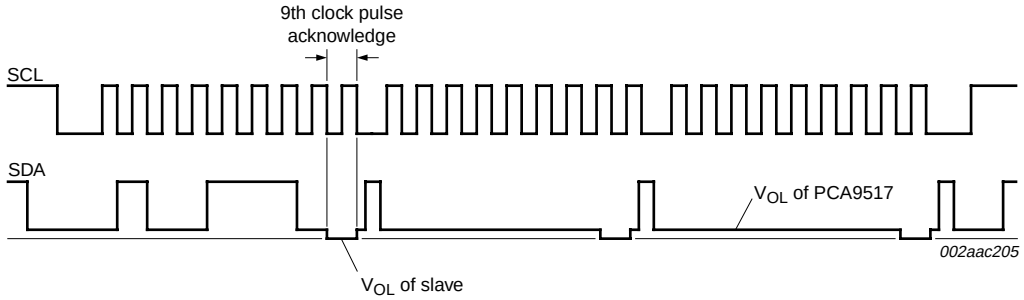


Fig 8. Bus B (2.7 V to 5.5 V) waveform

8. Limiting values

Table 3: Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CCB}	supply voltage, B side bus	2.7 V to 5.5 V	–0.5	+7	V
V_{CCA}	supply voltage, A side bus	adjustable	–0.5	+7	V
V_{bus}	voltage on I²C-bus B side, or enable (EN)		–0.5	+7	V
I	DC current	any pin	-	50	mA
P_{tot}	total power dissipation		-	100	mW
T_{stg}	storage temperature		–55	+125	°C
T_{amb}	ambient temperature	operating in free air	–40	+85	°C
T_j	junction temperature		-	+125	°C

9. Static characteristics

Table 4: Static characteristics

V_{CC} = 2.7 V to 5.5 V; GND = 0 V; T_{amb} = –40 °C to +85 °C; unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Supplies							
V_{CCB}	supply voltage, B side bus			2.7	-	5.5	V
V_{CCA}	supply voltage, A side bus		[1]	0.9	-	5.5	V
$I_{CC(VCCA)}$	supply current on pin V_{CCA}			-	-	1	mA
I_{CCH}	HIGH-state supply current	both channels HIGH; V_{CC} = 5.5 V; SDAn = SCLn = V_{CC}		-	1.5	5	mA
I_{CCL}	LOW-state supply current	both channels LOW; V_{CC} = 5.5 V; one SDA and one SCL = GND; other SDA and SCL open		-	1.5	5	mA
I_{CCAc}	quiescent supply current in contention	V_{CC} = 5.5 V; SDAn = SCLn = V_{CC}		-	1.5	5	mA
Input and output SDAB and SCLB							
V_{IH}	HIGH-level input voltage			0.7V_{CCB}	-	5.5	V
V_{IL}	LOW-level input voltage		[2]	–0.5	-	+0.3V_{CCB}	V
V_{ILc}	LOW-level input voltage contention			–0.5	0.4	-	V
V_{IK}	input clamping voltage	I_I = –18 mA		-	-	–1.2	V
I_{LI}	input leakage current	V_I = 3.6 V		-	-	±1	µA
I_{IL}	LOW-level input current	SDA, SCL; V_I = 0.2 V		-	-	10	µA
V_{OL}	LOW-level output voltage	I_{OL} = 100 µA or 6 mA		0.47	0.52	0.6	V
$V_{OL} – V_{ILc}$	LOW-level input voltage below output LOW-level voltage	guaranteed by design		-	-	70	mV
I_{LOH}	HIGH-level output leakage current	V_O = 3.6 V		-	-	10	µA
C_{io}	input/output capacitance	V_I = 3 V or 0 V; V_{CC} = 3.3 V		-	6	7	pF
		V_I = 3 V or 0 V; V_{CC} = 0 V		-	6	7	pF
Input and output SDAA and SCLA							
V_{IH}	HIGH-level input voltage			0.7V_{CCA}	-	5.5	V
V_{IL}	LOW-level input voltage			–0.5	-	+0.3V_{CCA}	V
V_{IK}	input clamping voltage	I_I = –18 mA		-	-	–1.2	V
I_{LI}	input leakage current	V_I = 3.6 V		-	-	±1	µA
I_{IL}	LOW-level input current	SDA, SCL; V_I = 0.2 V		-	-	10	µA
V_{OL}	LOW-level output voltage	I_{OL} = 6 mA		-	0.1	0.2	V
I_{LOH}	HIGH-level output leakage current	V_O = 3.6 V		-	-	10	µA
C_{io}	input/output capacitance	V_I = 3 V or 0 V; V_{CC} = 3.3 V		-	6	7	pF
		V_I = 3 V or 0 V; V_{CC} = 0 V		-	6	7	pF

Table 4: Static characteristics *...continued*

V_{CC} = 2.7 V to 5.5 V; GND = 0 V; T_{amb} = −40 °C to +85 °C; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Enable						
V_{IL}	LOW-level input voltage		−0.5	-	$+0.3V_{CCB}$	V
V_{IH}	HIGH-level input voltage		$0.7V_{CCB}$	-	5.5	V
$I_{IL(EN)}$	LOW-level input current on pin EN	V_I = 0.2 V, EN; V_{CC} = 3.6 V	-	−10	−30	µA
I_{LI}	input leakage current		−1	-	+1	µA
C_i	input capacitance	V_I = 3.0 V or 0 V	-	6	7	pF

[1] LOW-level supply voltage.

[2] V_{IL} specification is for the first LOW level seen by the SDAB/SCLB lines. V_{ILc} is for the second and subsequent LOW levels seen by the SDAB/SCLB lines.

10. Dynamic characteristics

Table 5: Dynamic characteristics

V_{CC} = 2.7 V to 5.5 V; GND = 0 V; T_{amb} = −40 °C to +85 °C; unless otherwise specified. [1] [2]

Symbol	Parameter	Conditions		Min	Typ [3]	Max	Unit
t_{PLH}	LOW-to-HIGH propagation delay	B side to A side; Figure 11	[4]	100	170	250	ns
t_{PHL}	HIGH-to-LOW propagation delay	B side to A side; Figure 9					
		$V_{CCA} \leq 2.7$ V	[5]	30	80	110	ns
		$V_{CCA} \geq 3$ V		10	66	300	ns
$t_{t(LH)}$	LOW-to-HIGH transition time	A side; Figure 10		10	20	30	ns
$t_{t(HL)}$	HIGH-to-LOW transition time	A side; Figure 10					
		$V_{CCA} \leq 2.7$ V	[5]	1	77	105	ns
		$V_{CCA} \geq 3$ V		20	70	175	ns
t_{PLH}	LOW-to-HIGH propagation delay	A side to B side; Figure 10	[6]	25	53	110	ns
t_{PHL}	HIGH-to-LOW propagation delay	A side to B side; Figure 10	[6]	60	79	230	ns
$t_{t(LH)}$	LOW-to-HIGH transition time	B side; Figure 9		120	140	170	ns
$t_{t(HL)}$	HIGH-to-LOW transition time	B side; Figure 9		30	48	90	ns
t_{su}	setup time	EN HIGH before START condition	[7]	100	-	-	ns
t_h	hold time	EN HIGH after STOP condition	[7]	100	-	-	ns

[1] Times are specified with loads of 1.35 kΩ pull-up resistance and 57 pF load capacitance on the B side, and 167 Ω pull-up resistance and 57 pF load capacitance on the A side. Different load resistance and capacitance will alter the RC time constant, thereby changing the propagation delay and transition times.

[2] Pull-up voltages are V_{CCA} on the A side and V_{CCB} on the B side.

[3] Typical values were measured with V_{CCA} = 3.3 V at T_{amb} = 25 °C, unless otherwise noted.

[4] The t_{PLH} delay data from B side to A side is measured at 0.5 V on the B side to $0.5V_{CCA}$ on the A side when V_{CCA} is less than 2 V, and 1.5 V on the A side if V_{CCA} is greater than 2 V.

[5] Typical value measured with V_{CCA} = 2.7 V at T_{amb} = 25 °C.

[6] The proportional delay data from A side to B side is measured at $0.3V_{CCA}$ on the A side to 1.5 V on the B side.

[7] The enable pin, EN, should only change state when the global bus and the repeater port are in an idle state.

10.1 AC waveforms

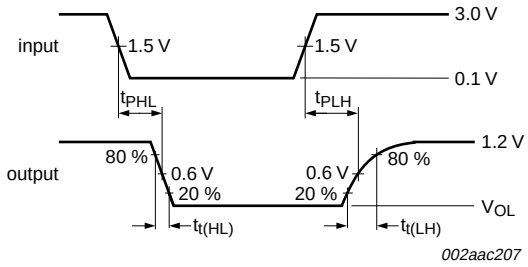


Fig 9. Propagation delay and transition times; B side to A side

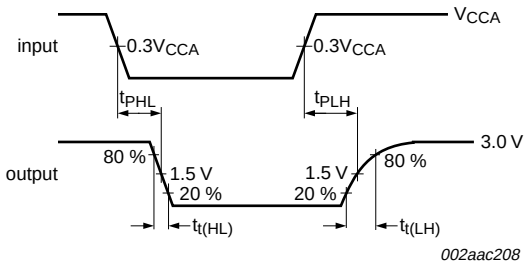


Fig 10. Propagation delay and transition times; A side to B side

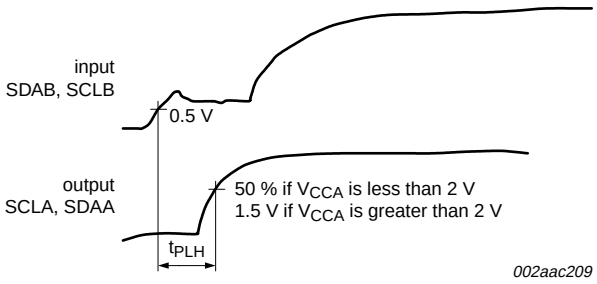
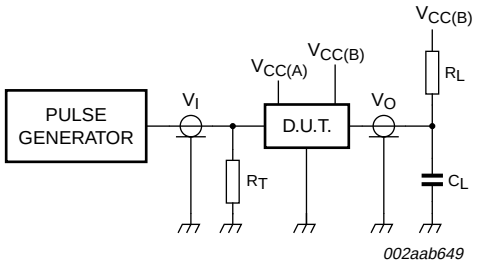


Fig 11. Propagation delay

11. Test information



R_L = load resistor; 1.35 kΩ on B side; 167 Ω on A side

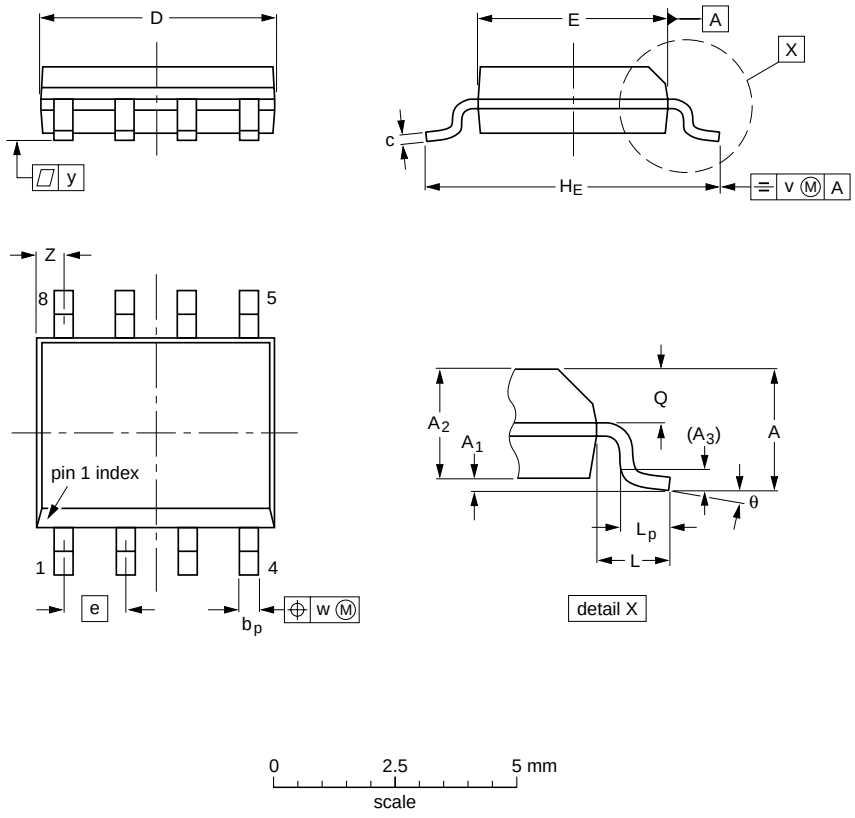
C_L = load capacitance includes jig and probe capacitance; 57 pF

R_T = termination resistance should be equal to Z_o of pulse generators

Fig 12. Test circuit for open-drain outputs

12. Package outline

SO8: plastic small outline package; 8 leads; body width 3.9 mm **SOT96-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(2)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	1.75	0.25 0.10	1.45 1.25	0.25	0.49 0.36	0.25 0.19	5.0 4.8	4.0 3.8	1.27	6.2 5.8	1.05	1.0 0.4	0.7 0.6	0.25	0.25	0.1	0.7 0.3	8^o 0^o
inches	0.069	0.010 0.004	0.057 0.049	0.01	0.019 0.014	0.0100 0.0075	0.20 0.19	0.16 0.15	0.05	0.244 0.228	0.041	0.039 0.016	0.028 0.024	0.01	0.01	0.004	0.028 0.012	

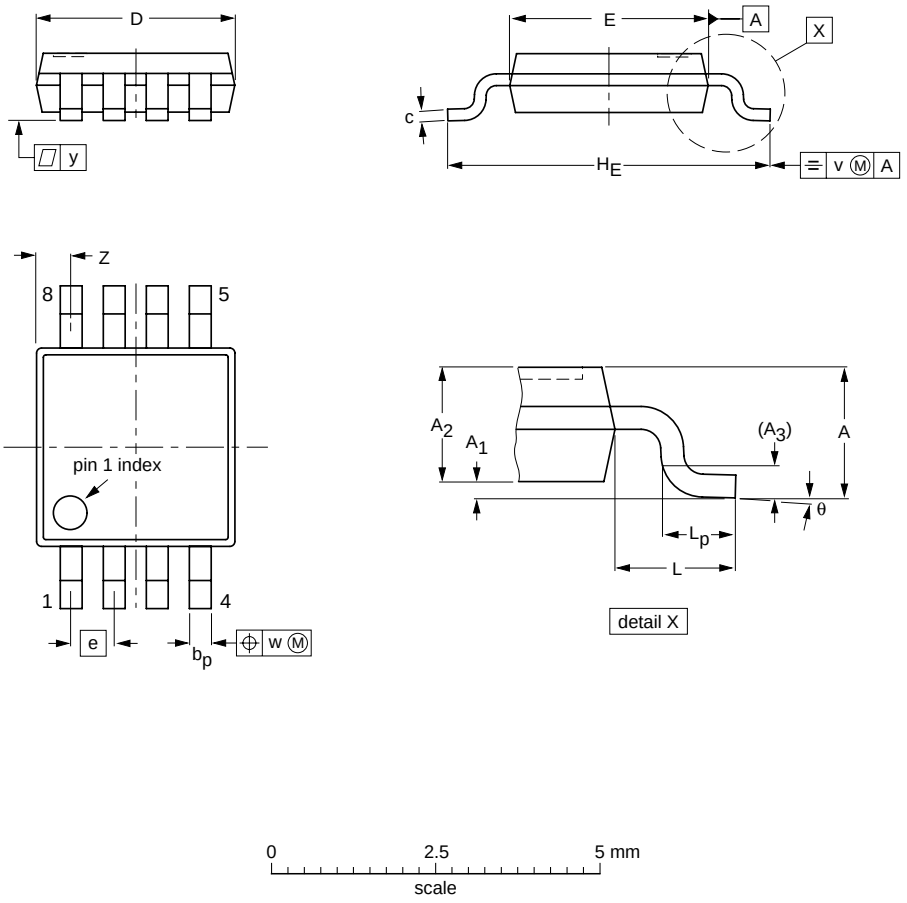
Notes

1. Plastic or metal protrusions of 0.15 mm (0.006 inch) maximum per side are not included.
2. Plastic or metal protrusions of 0.25 mm (0.01 inch) maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT96-1	076E03	MS-012				~~99-12-27~~ 03-02-18

Fig 13. Package outline SOT96-1 (SO8)

TSSOP8: plastic thin shrink small outline package; 8 leads; body width 3 mm **SOT505-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(2)}$	e	H_E	L	L_p	v	w	y	$Z^{(1)}$	θ
mm	1.1	0.15 0.05	0.95 0.80	0.25	0.45 0.25	0.28 0.15	3.1 2.9	3.1 2.9	0.65	5.1 4.7	0.94	0.7 0.4	0.1	0.1	0.1	0.70 0.35	6° 0°

Notes

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT505-1						~~99-04-09~~ 03-02-18

Fig 14. Package outline SOT505-1 (TSSOP8)

13. Soldering

13.1 Introduction to soldering surface mount packages

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in our *Data Handbook IC26; Integrated Circuit Packages* (document order number 9398 652 90011).

There is no soldering method that is ideal for all surface mount IC packages. Wave soldering can still be used for certain surface mount ICs, but it is not suitable for fine pitch SMDs. In these situations reflow soldering is recommended.

13.2 Reflow soldering

Reflow soldering requires solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the printed-circuit board by screen printing, stencilling or pressure-syringe dispensing before package placement. Driven by legislation and environmental forces the worldwide use of lead-free solder pastes is increasing.

Several methods exist for reflowing; for example, convection or convection/infrared heating in a conveyor type oven. Throughput times (preheating, soldering and cooling) vary between 100 seconds and 200 seconds depending on heating method.

Typical reflow peak temperatures range from 215 °C to 270 °C depending on solder paste material. The top-surface temperature of the packages should preferably be kept:

- below 225 °C (SnPb process) or below 245 °C (Pb-free process)
  - for all BGA, HTSSON..T and SSOP..T packages
  - for packages with a thickness ≥ 2.5 mm
  - for packages with a thickness < 2.5 mm and a volume ≥ 350 mm^3 so called thick/large packages.
- below 240 °C (SnPb process) or below 260 °C (Pb-free process) for packages with a thickness < 2.5 mm and a volume < 350 mm^3 so called small/thin packages.

Moisture sensitivity precautions, as indicated on packing, must be respected at all times.

13.3 Wave soldering

Conventional single wave soldering is not recommended for surface mount devices (SMDs) or printed-circuit boards with a high component density, as solder bridging and non-wetting can present major problems.

To overcome these problems the double-wave soldering method was specifically developed.

If wave soldering is used the following conditions must be observed for optimal results:

- Use a double-wave soldering method comprising a turbulent wave with high upward pressure followed by a smooth laminar wave.
- For packages with leads on two sides and a pitch (e):
  - larger than or equal to 1.27 mm, the footprint longitudinal axis is **preferred** to be parallel to the transport direction of the printed-circuit board;

– smaller than 1.27 mm, the footprint longitudinal axis **must** be parallel to the transport direction of the printed-circuit board.

The footprint must incorporate solder thieves at the downstream end.

- For packages with leads on four sides, the footprint must be placed at a 45° angle to the transport direction of the printed-circuit board. The footprint must incorporate solder thieves downstream and at the side corners.

During placement and before soldering, the package must be fixed with a droplet of adhesive. The adhesive can be applied by screen printing, pin transfer or syringe dispensing. The package can be soldered after the adhesive is cured.

Typical dwell time of the leads in the wave ranges from 3 seconds to 4 seconds at 250 °C or 265 °C, depending on solder material applied, SnPb or Pb-free respectively.

A mildly-activated flux will eliminate the need for removal of corrosive residues in most applications.

13.4 Manual soldering

Fix the component by first soldering two diagonally-opposite end leads. Use a low voltage (24 V or less) soldering iron applied to the flat part of the lead. Contact time must be limited to 10 seconds at up to 300 °C.

When using a dedicated tool, all other leads can be soldered in one operation within 2 seconds to 5 seconds between 270 °C and 320 °C.

13.5 Package related soldering information

Table 6: Suitability of surface mount IC packages for wave and reflow soldering methods

Package [1]	Soldering method	
	Wave	Reflow [2]
BGA, HTSSON..T [3], LBGA, LFBGA, SQFP, SSOP..T [3], TFBGA, VFBGA, XSON	not suitable	suitable
DHVQFN, HBCC, HBGA, HLQFP, HSO, HSOP, HSQFP, HSSON, HTQFP, HTSSOP, HVQFN, HVSON, SMS	not suitable [4]	suitable
PLCC [5], SO, SOJ	suitable	suitable
LQFP, QFP, TQFP	not recommended [5] [6]	suitable
SSOP, TSSOP, VSO, VSSOP	not recommended [7]	suitable
CWQCCN..L [8], PMFP [9], WQCCN..L [8]	not suitable	not suitable

[1] For more detailed information on the BGA packages refer to the *(LF)BGA Application Note* (AN01026); order a copy from your Philips Semiconductors sales office.

[2] All surface mount (SMD) packages are moisture sensitive. Depending upon the moisture content, the maximum temperature (with respect to time) and body size of the package, there is a risk that internal or external package cracks may occur due to vaporization of the moisture in them (the so called popcorn effect). For details, refer to the Drypack information in the *Data Handbook IC26; Integrated Circuit Packages; Section: Packing Methods*.

[3] These transparent plastic packages are extremely sensitive to reflow soldering conditions and must on no account be processed through more than one soldering cycle or subjected to infrared reflow soldering with peak temperature exceeding 217 °C ± 10 °C measured in the atmosphere of the reflow oven. The package body peak temperature must be kept as low as possible.

[4] These packages are not suitable for wave soldering. On versions with the heatsink on the bottom side, the solder cannot penetrate between the printed-circuit board and the heatsink. On versions with the heatsink on the top side, the solder might be deposited on the heatsink surface.

[5] If wave soldering is considered, then the package must be placed at a 45° angle to the solder wave direction. The package footprint must incorporate solder thieves downstream and at the side corners.

[6] Wave soldering is suitable for LQFP, QFP and TQFP packages with a pitch (e) larger than 0.8 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.65 mm.

[7] Wave soldering is suitable for SSOP, TSSOP, VSO and VSSOP packages with a pitch (e) equal to or larger than 0.65 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.5 mm.

[8] Image sensor packages in principle should not be soldered. They are mounted in sockets or delivered pre-mounted on flex foil. However, the image sensor package can be mounted by the client on a flex foil by using a hot bar soldering process. The appropriate soldering profile can be provided on request.

[9] Hot bar soldering or manual soldering is suitable for PMFP packages.

14. Abbreviations

Table 7: Abbreviations

Acronym	Description
CDM	Charged Device Model
CMOS	Complementary Metal Oxide Silicon
ESD	ElectroStatic Discharge
HBM	Human Body Model
I²C-bus	Inter Integrated Circuit bus
MM	Machine Model
SMBus	System Management Bus

15. Revision history

Table 8: Revision history

Document ID	Release date	Data sheet status	Change notice	Doc. number	Supersedes
PCA9517_2	20060615	Product data sheet	-	9397 750 14918	PCA9517_1
Modifications:	• The format of this data sheet has been redesigned to comply with the new presentation and information standard of Philips Semiconductors. • Section 2 “Features”, 11th bullet re-written • Table 2 “Pin description”: changed description of pin V_{CCB} from “2.7 V to 3.6 V” to “2.7 V to 5.5 V” • Table 3 “Limiting values”: changed descriptions of symbols V_{CCB}, V_{CCA} • Table 4 “Static characteristics”: – changed description line below title from “V_{CC} = 2.7 V to 3.6 V” to “V_{CC} = 2.7 V to 5.5 V” – under subsection “Supplies”: changed descriptions of symbols V_{CCB}, V_{CCA}, I_{CC}, I_{CCH}; changed symbol “I_{CCA}” to “I_{CCL}” – added (new) Table note 1 and its reference at V_{CCA} – changed maximum value for V_{CCB} from 3.6 V to 5.5 V – values for I_{CCAH}, I_{CCBH}, I_{CCAc} updated – changed “V_{CC} = 3.6 V” to “V_{CC} = 5.5 V” under Conditions for I_{CCH}, I_{CCL} and I_{CCAc} parameters – under subsection “Input and output SDAB and SCLB”: changed symbol “I_I” to “I_{LI}”; changed description of symbol I_{IL}; changed symbol I_{OH} to I_{LOH} and modified its description. – removed reference to Table note 2 (old Note 1) from V_{IL} under sub-section “Input and output SDAA and SCLA” – under subsection “Input and output SDAA and SCLA”: changed symbol “I_I” to “I_{LI}”; changed description of symbol I_{IL}; changed symbol I_{OH} to I_{LOH} and modified its description. – Table note 2: changed “SDAx/SCLx” to “SDAB/SCLB” (2 places) – under subsection “Enable”, changed symbol I_{IL} to $I_{IL(EN)}$; changed Typ and Max values to negative numbers • Table 5 “Dynamic characteristics”: – reordered sequence of table notes – symbol t_{TLH} changed to $t_{t(LH)}$ – symbol t_{HL} changed to $t_{t(HL)}$ – symbol t_{SET} changed to t_{su} – symbol t_{HOLD} changed to t_h • Figure 9 and Figure 10: changed “3.3 V” to “3.0 V”				
PCA9517_1	20041005	Product data sheet	-	9397 750 13252	-

16. Data sheet status

Level	Data sheet status [1]	Product status [2] [3]	Definition
I	Objective data	Development	This data sheet contains data from the objective specification for product development. Philips Semiconductors reserves the right to change the specification in any manner without notice.
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[3] For data sheets describing multiple type numbers, the highest-level product status determines the data sheet status.

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Short-form specification — The data in a short-form specification is extracted from a full data sheet with the same type number and title. For detailed information see the relevant data sheet or data handbook.

Limiting values definition — Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 60134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

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21. Contents

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