DATA SHEET

PCA9545A

4-channel I^2C switch with interrupt logic and reset

Objective data sheet
Supersedes data of 2004 Jul 28

2004 Sep 29

Philips
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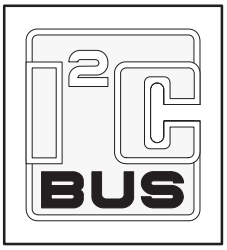
4-channel I²C switch with interrupt logic and reset PCA9545A



FEATURES

- 1-of-4 bi-directional translating switches
- I²C interface logic; compatible with SMBus standards
- 4 active-LOW interrupt inputs
- Active-LOW interrupt output
- Active-LOW reset input
- 2 address pins allowing up to 4 devices on the I²C-bus
- Channel selection via I²C-bus, in any combination
- Power-up with all switch channels deselected
- Low RDS_{ON} switches
- Allows voltage level translation between 1.8 V, 2.5 V, 3.3 V and 5 V buses
- No glitch on power-up
- Supports hot insertion
- Low stand-by current
- Operating power supply voltage range of 2.3 V to 5.5 V
- 5 V tolerant Inputs
- 0 kHz to 400 kHz clock frequency
- ESD protection exceeds 2000 V HBM per JESD22-A114, 200 V MM per JESD22-A115 and 1000 V per JESD22-C101
- Latch-up testing is done to JESDEC Standard JESD78 which exceeds 100 mA
- Three packages offered: SO20, TSSOP20, and HVQFN20

DESCRIPTION

The PCA9545A is a quad bi-directional translating switch controlled via the I²C-bus. The SCL/SDA upstream pair fans out to four downstream pairs, or channels. Any individual SCx/SDx channel or combination of channels can be selected, determined by the contents of the programmable control register. Four interrupt inputs, $\overline{INT0}$ to $\overline{INT3}$, one for each of the downstream pairs, are provided. One interrupt output, $\overline{INT}$, acts as an AND of the four interrupt inputs.

An active-LOW reset input allows the PCA9545A to recover from a situation where one of the downstream I²C-buses is stuck in a LOW state. Pulling the $\overline{RESET}$ pin LOW resets the I²C state machine and causes all the channels to be deselected as does the internal Power-On Reset function.

The pass gates of the switches are constructed such that the V_{DD} pin can be used to limit the maximum high voltage which will be passed by the PCA9545A. This allows the use of different bus voltages on each pair, so that 1.8 V or 2.5 V or 3.3 V parts can communicate with 5 V parts without any additional protection. External pull-up resistors pull the bus up to the desired voltage level for each channel. All I/O pins are 5 V tolerant.

ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	ORDER CODE	TOPSIDE MARKING	DRAWING NUMBER
20-Pin Plastic SO	–40 °C to +85 °C	PCA9545AD	PCA9545AD	SOT163-1
20-Pin Plastic TSSOP	–40 °C to +85 °C	PCA9545APW	PA9545A	SOT360-1
20-Pin Plastic HVQFN	–40 °C to +85 °C	PCA9545ABS	9545A	SOT662-1

Standard packing quantities and other packaging data are available at www.standardproducts.philips.com/packaging.

PIN CONFIGURATION — SO, TSSOP

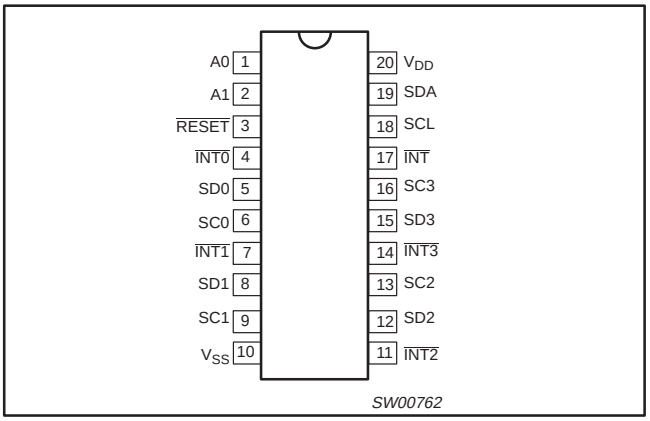


Figure 1. Pin configuration — SO, TSSOP

PIN CONFIGURATION — HVQFN

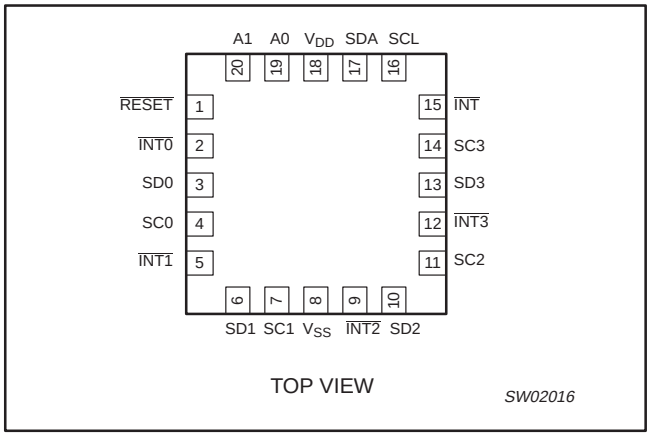


Figure 2. Pin configuration — HVQFN

PIN DESCRIPTION

SO, TSSOP PIN NUMBER	HVQFN PIN NUMBER	SYMBOL	FUNCTION
1	19	A0	Address input 0
2	20	A1	Address input 1
3	1	$\overline{\text{RESET}}$	Active-LOW reset input
4	2	$\overline{\text{INT0}}$	Active-LOW interrupt input 0
5	3	SD0	Serial data 0
6	4	SC0	Serial clock 0
7	5	$\overline{\text{INT1}}$	Active-LOW interrupt input 1
8	6	SD1	Serial data 1
9	7	SC1	Serial clock 1
10	8	V_{SS}	Supply ground
11	9	$\overline{\text{INT2}}$	Active-LOW interrupt input 2
12	10	SD2	Serial data 2
13	11	SC2	Serial clock 2
14	12	$\overline{\text{INT3}}$	Active-LOW interrupt input 3
15	13	SD3	Serial data 3
16	14	SC3	Serial clock 3
17	15	$\overline{\text{INT}}$	Active-LOW interrupt output
18	16	SCL	Serial clock line
19	17	SDA	Serial data line
20	18	V_{DD}	Supply voltage

BLOCK DIAGRAM

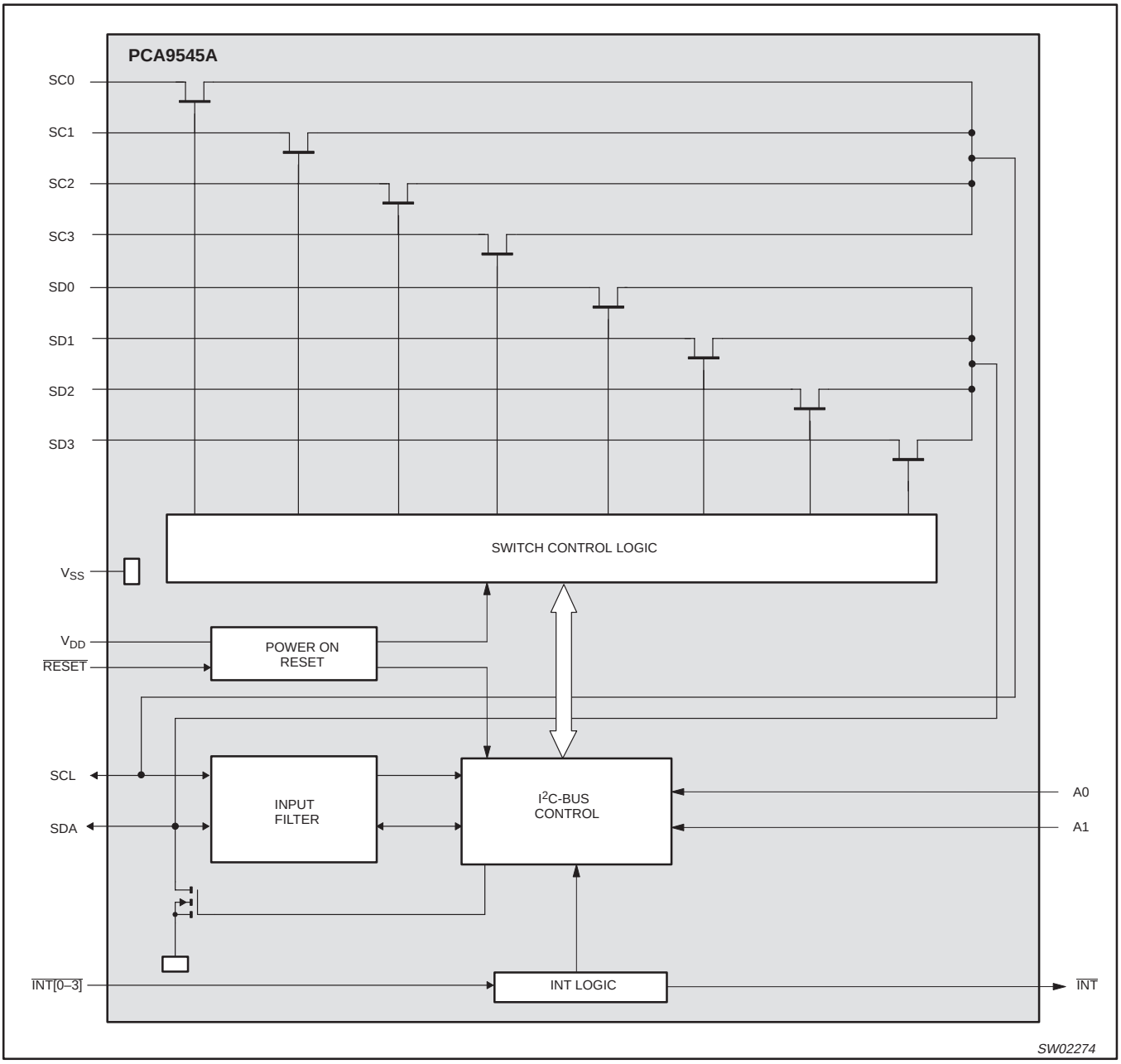


Figure 3. Block diagram

DEVICE ADDRESS

Following a START condition the bus master must output the address of the slave it is accessing. The address of the PCA9545A is shown in Figure 4. To conserve power, no internal pullup resistors are incorporated on the hardware selectable address pins and they must be pulled HIGH or LOW.

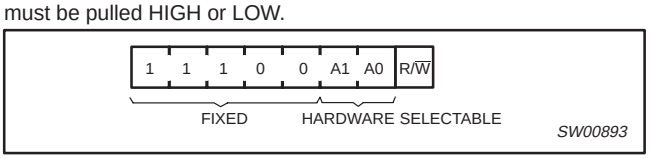


Figure 4. Slave address

The last bit of the slave address defines the operation to be performed. When set to logic 1, a read is selected while a logic 0 selects a write operation.

CONTROL REGISTER

Following the successful acknowledgement of the slave address, the bus master will send a byte to the PCA9545A, which will be stored in the control register. If multiple bytes are received by the PCA9545A, it will save the last byte received. This register can be written and read via the I²C-bus.

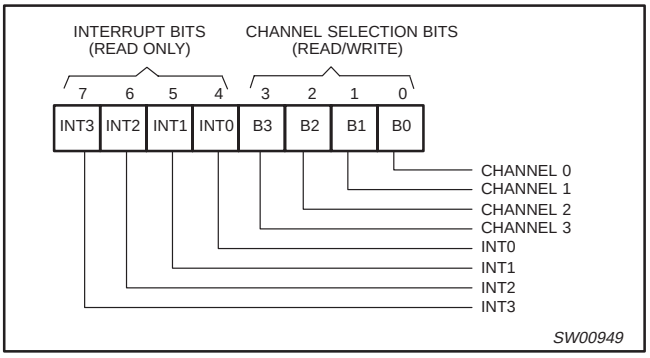


Figure 5. Control Register

CONTROL REGISTER DEFINITION

One or several SCx/SDx downstream pair, or channel, is selected by the contents of the control register. This register is written after the PCA9545A has been addressed. The 4 LSBs of the control byte are used to determine which channel is to be selected. When a channel is selected, the channel will become active after a stop condition has been placed on the I²C-bus. This ensures that all SCx/SDx lines will be in a HIGH state when the channel is made active, so that no false conditions are generated at the time of connection.

Table 1. Control Register; Write — Channel Selection/ Read — Channel Status

INT3	INT2	INT1	INT0	B3	B2	B1	B0	COMMAND
X	X	X	X	X	X	X	0	Channel 0 disabled
							1	Channel 0 enabled
X	X	X	X	X	X	0	X	Channel 1 disabled
						1		Channel 1 enabled
X	X	X	X	X	0	X	X	Channel 2 disabled
					1			Channel 2 enabled
X	X	X	X	0	X	X	X	Channel 3 disabled
				1				Channel 3 enabled
0	0	0	0	0	0	0	0	No channel selected; power-up/ reset default state

NOTE: Several channels can be enabled at the same time.
Ex: B3 = 0, B2 = 1, B1 = 1, B0 = 0, means that channel 0 and 3 are disabled and channel 1 and 2 are enabled.
Care should be taken not to exceed the maximum bus capacity.

INTERRUPT HANDLING

The PCA9545A provides 4 interrupt inputs, one for each channel, and one open drain interrupt output. When an interrupt is generated by any device, it will be detected by the PCA9545A and the interrupt output will be driven LOW. The channel does not need to be active for detection of the interrupt. A bit is also set in the control register.

Bits 4 – 7 of the control register correspond to channels 0 – 3 of the PCA9545A, respectively. Therefore, if an interrupt is generated by any device connected to channel 1, the state of the interrupt inputs is loaded into the control register when a read is accomplished. Likewise, an interrupt on any device connected to channel 0 would cause bit 4 of the control register to be set on the read. The master can then address the PCA9545A and read the contents of the control register to determine which channel contains the device generating the interrupt. The master can then reconfigure the PCA9545A to select this channel, and locate the device generating the interrupt and clear it.

It should be noted that more than one device can be providing an interrupt on a channel, so it is up to the master to ensure that all devices on a channel are interrogated for an interrupt.

The interrupt inputs may be used as general purpose inputs if the interrupt function is not required.

If unused, interrupt input(s) must be connected to V_{DD} through a pull-up resistor.

Table 2. Control Register Read — Interrupt

INT3	INT2	INT1	INT0	B3	B2	B1	B0	COMMAND
X	X	X	0	X	X	X	X	No interrupt on channel 0
			1					Interrupt on channel 0
X	X	0		X	X	X	X	No interrupt on channel 1
		1						Interrupt on channel 1
X	0	X		X	X	X	X	No interrupt on channel 2
	1							Interrupt on channel 2
0	X	X		X	X	X	X	No interrupt on channel 3
1								Interrupt on channel 3

NOTE: Several interrupts can be active at the same time.
Ex: INT3 = 0, INT2 = 1, INT1 = 1, INT0 = 0, means that there is no interrupt on channels 0 and 3, and there is interrupt on channels 1 and 2.

$\overline{\text{RESET}}$ INPUT

The $\overline{\text{RESET}}$ input is an active-LOW signal which may be used to recover from a bus fault condition. By asserting this signal LOW for a minimum of t_{WL}, the PCA9545A will reset its registers and I²C state machine and will deselect all channels. The $\overline{\text{RESET}}$ input must be connected to V_{DD} through a pull-up resistor.

POWER-ON RESET

When power is applied to V_{DD}, an internal Power-On Reset holds the PCA9545A in a reset condition until V_{DD} has reached V_{POR}. At this point, the reset condition is released and the PCA9545A registers and I²C state machine are initialized to their default states, all zeroes causing all the channels to be deselected. Thereafter, V_{DD} must be lowered below 0.2 V to reset the device.

VOLTAGE TRANSLATION

The pass gate transistors of the PCA9545A are constructed such that the V_{DD} voltage can be used to limit the maximum voltage that will be passed from one I²C-bus to another.

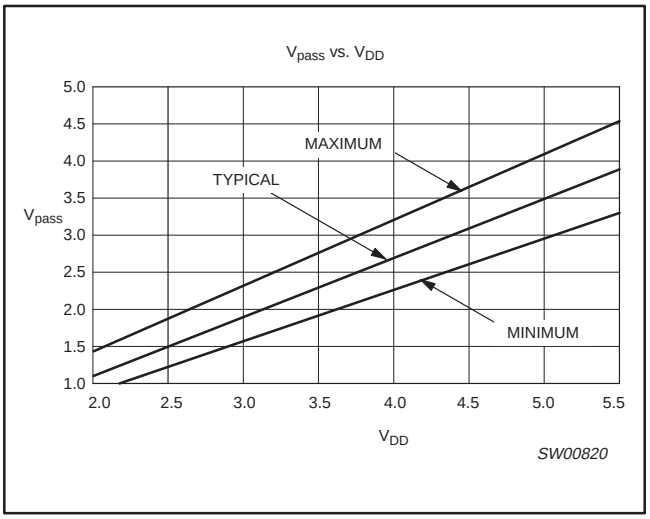


Figure 6. V_{pass} voltage vs. V_{DD}

Figure 6 shows the voltage characteristics of the pass gate transistors (note that the graph was generated using the data specified in the DC Characteristics section of this datasheet). In order for the PCA9545A to act as a voltage translator, the V_{pass} voltage should be equal to, or lower than the lowest bus voltage. For example, if the main bus was running at 5 V, and the downstream buses were 3.3 V and 2.7 V, then V_{pass} should be equal to or below 2.7 V to effectively clamp the downstream bus voltages. Looking at Figure 6, we see that V_{pass} (max.) will be at 2.7 V when the PCA9545A supply voltage is 3.5 V or lower so the PCA9545A supply voltage could be set to 3.3 V. Pull-up resistors can then be used to bring the bus voltages to their appropriate levels (see Figure 13).

More Information can be found in Application Note AN262 *PCA954X family of I²C/SMBus multiplexers and switches.*

CHARACTERISTICS OF THE I²C-BUS

The I²C-bus is for 2-way, 2-line communication between different ICs or modules. The two lines are a serial data line (SDA) and a serial clock line (SCL). Both lines must be connected to a positive supply via a pull-up resistor when connected to the output stages of a device. Data transfer may be initiated only when the bus is not busy.

Bit transfer

One data bit is transferred during each clock pulse. The data on the SDA line must remain stable during the HIGH period of the clock pulse as changes in the data line at this time will be interpreted as control signals (see Figure 7).

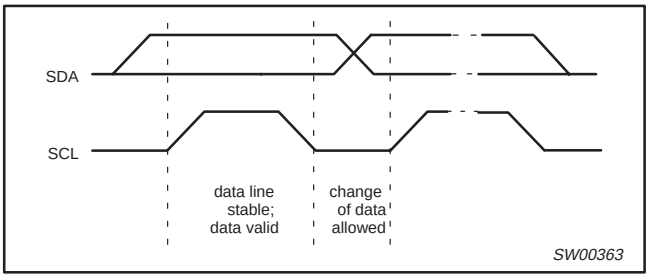


Figure 7. Bit transfer

Start and stop conditions

Both data and clock lines remain HIGH when the bus is not busy. A HIGH-to-LOW transition of the data line, while the clock is HIGH is defined as the start condition (S). A LOW-to-HIGH transition of the data line while the clock is HIGH is defined as the stop condition (P) (see Figure 8).

System configuration

A device generating a message is a ‘transmitter’, a device receiving is the ‘receiver’. The device that controls the message is the ‘master’ and the devices which are controlled by the master are the ‘slaves’ (see Figure 9).

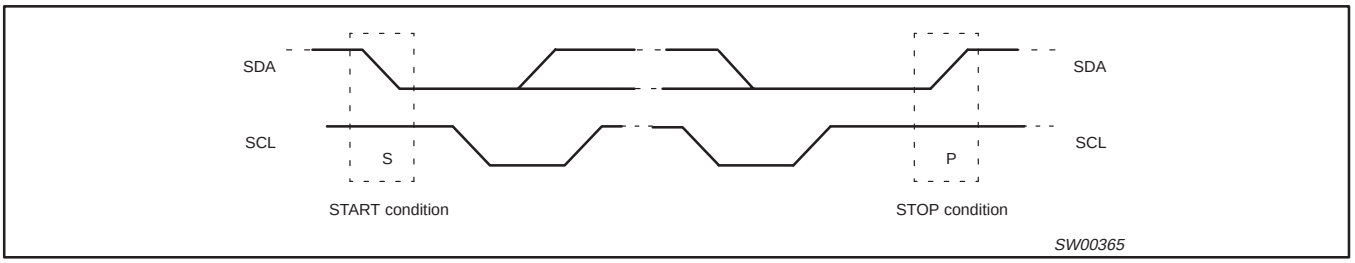


Figure 8. Definition of start and stop conditions

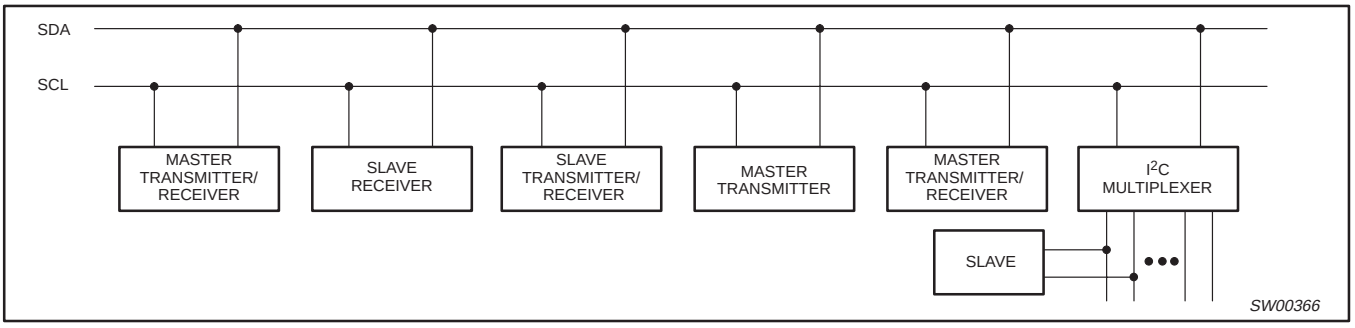


Figure 9. System configuration

Acknowledge

The number of data bytes transferred between the start and the stop conditions from transmitter to receiver is not limited. Each byte of eight bits is followed by one acknowledge bit. The acknowledge bit is a HIGH level put on the bus by the transmitter whereas the master generates an extra acknowledge related clock pulse.

A slave receiver which is addressed must generate an acknowledge after the reception of each byte. Also a master must generate an acknowledge after the reception of each byte that has been clocked out of the slave transmitter. The device that acknowledges has to pull down the SDA line during the acknowledge clock pulse, so that the SDA line is stable LOW during the HIGH period of the acknowledge related clock pulse, set-up and hold times must be taken into account.

A master receiver must signal an end of data to the transmitter by not generating an acknowledge on the last byte that has been clocked out of the slave. In this event, the transmitter must leave the data line HIGH to enable the master to generate a stop condition.

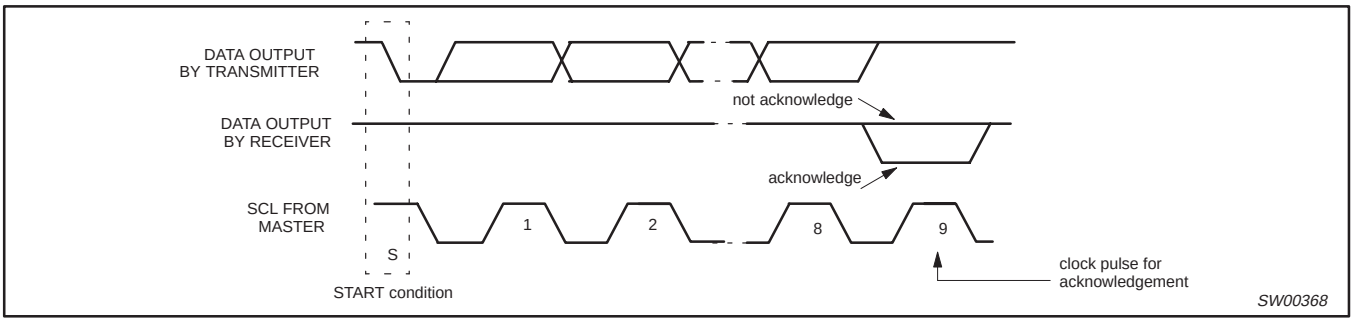


Figure 10. Acknowledgement on the I²C-bus

Bus transactions

Data is transmitted to the PCA9545A control register using the write mode as shown in Figure 11.

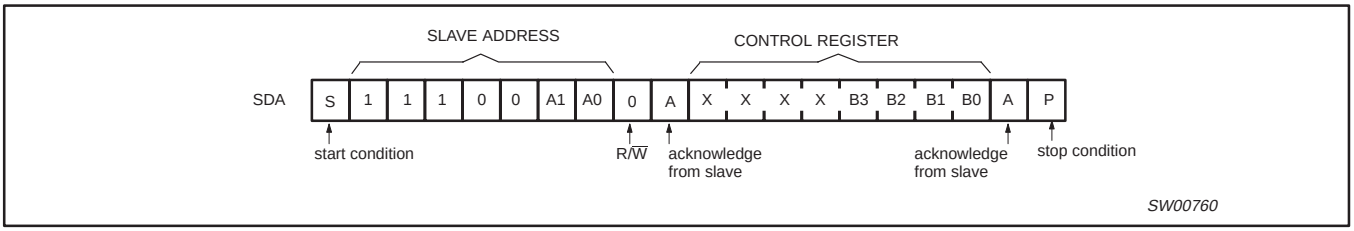


Figure 11. WRITE control register

Data is read from PCA9545A control register using the read mode as shown in Figure 12.

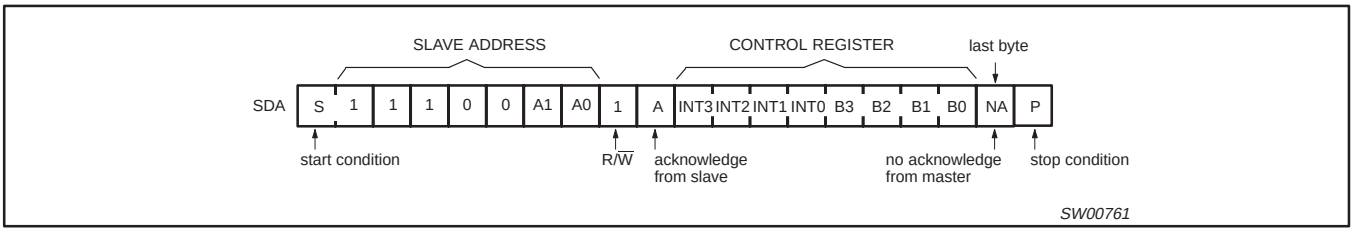
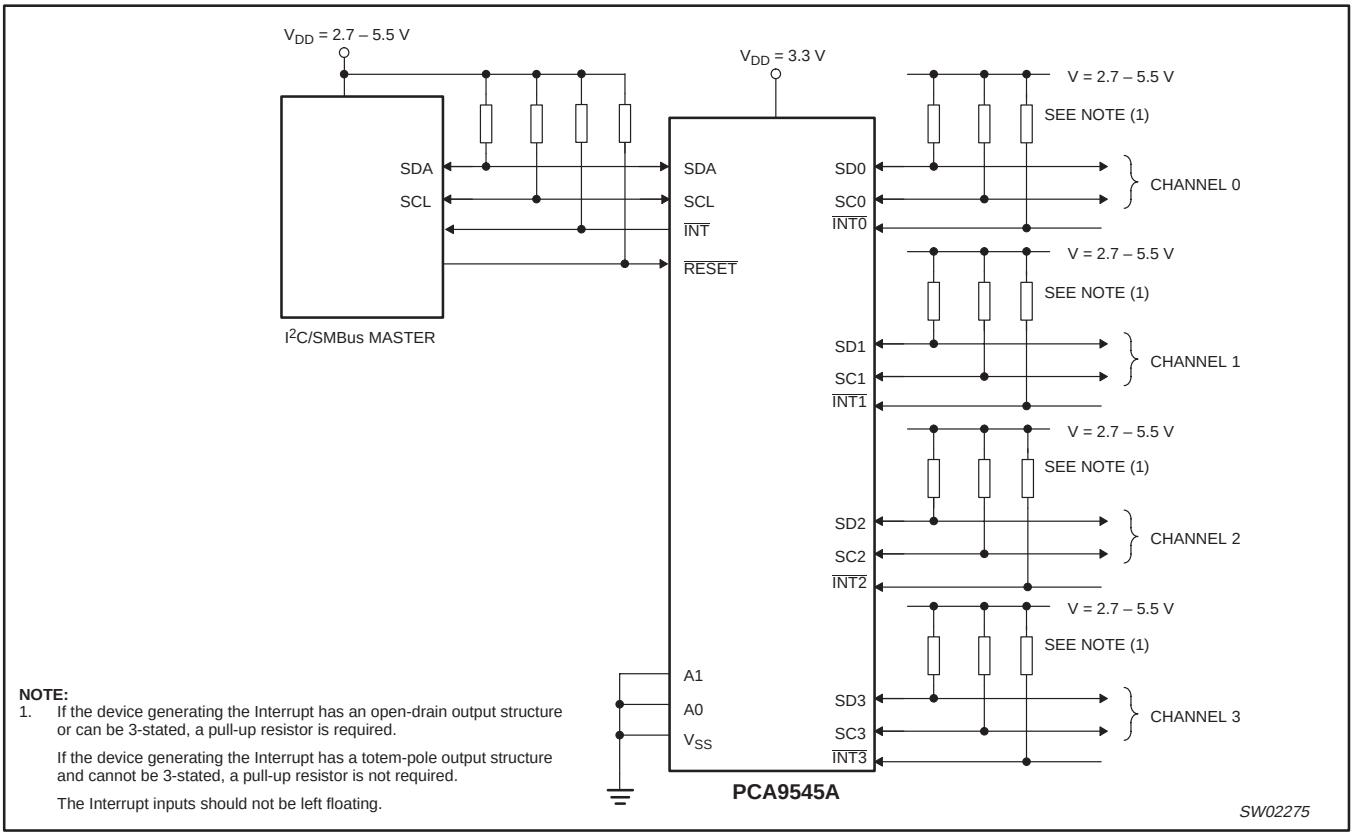


Figure 12. READ control register

TYPICAL APPLICATION



NOTE:
1. If the device generating the Interrupt has an open-drain output structure or can be 3-stated, a pull-up resistor is required.

   If the device generating the Interrupt has a totem-pole output structure and cannot be 3-stated, a pull-up resistor is not required.

   The Interrupt inputs should not be left floating.

Figure 13. Typical application

ABSOLUTE MAXIMUM RATINGS[1, 2]

In accordance with the Absolute Maximum Rating System (IEC 134).Voltages are referenced to GND (ground = 0 V).

SYMBOL	PARAMETER	CONDITIONS	RATING		UNIT
			MIN	MAX	
V_{DD}	DC supply voltage		–0.5	+7.0	V
V_I	DC input voltage		–0.5	+7.0	V
I_I	DC input current		—	±20	mA
I_O	DC output current		—	±25	mA
I_{DD}	DC Supply current		—	±100	mA
I_{SS}	DC Supply current		—	±100	mA
P_{tot}	total power dissipation		—	400	mW
T_{stg}	Storage temperature range		–60	+150	°C
T_{amb}	Operating ambient temperature		–40	+85	°C

NOTES:
1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The performance capability of a high-performance integrated circuit in conjunction with its thermal environment can create junction temperatures which are detrimental to reliability. The maximum junction temperature of this integrated circuit should not exceed 150 °C.

DC CHARACTERISTICS

V_{DD} = 2.3 V to 3.6 V; V_{SS} = 0 V; T_{amb} = –40 °C to +85 °C; unless otherwise specified. (See page 11 for V_{DD} = 4.5 V to 5.5 V.)

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			MIN	TYP	MAX	
Supply						
V_{DD}	Supply voltage		2.3	—	3.6	V
I_{DD}	Supply current	Operating mode; V_{DD} = 3.6 V; no load; V_I = V_{DD} or V_{SS}; f_{SCL} = 100 kHz	—	10	30	µA
I_{stb}	Standby current	Standby mode; V_{DD} = 3.6 V; no load; V_I = V_{DD} or V_{SS}	—	0.1	1	µA
V_{POR}	Power-on reset voltage (Note 1)	no load; V_I = V_{DD} or V_{SS}	—	1.6	2.1	V
Input SCL; input/output SDA						
V_{IL}	LOW-level input voltage		–0.5	—	$0.3V_{DD}$	V
V_{IH}	HIGH-level input voltage		$0.7V_{DD}$	—	6	V
I_{OL}	LOW-level output current	V_{OL} = 0.4 V	3	7	—	mA
		V_{OL} = 0.6 V	6	10	—	
I_L	Leakage current	V_I = V_{DD} or V_{SS}	–1	—	+1	µA
C_i	Input capacitance	V_I = V_{SS}	—	10	13	pF
Select inputs A0 to A1 / $\overline{\text{INT0}}$ to $\overline{\text{INT3}}$ / $\overline{\text{RESET}}$						
V_{IL}	LOW-level input voltage		–0.5	—	$0.3V_{DD}$	V
V_{IH}	HIGH-level input voltage		$0.7V_{DD}$	—	V_{DD} + 0.5	V
I_{LI}	Input leakage current	pin at V_{DD} or V_{SS}	–1	—	+1	µA
C_i	Input capacitance	V_I = V_{SS}	—	1.6	3	pF
Pass Gate						
R_{ON}	Switch resistance	V_{DD} = 3.0 V to 3.6 V; V_O = 0.4 V; I_O = 15 mA	5	11	30	Ω
		V_{DD} = 2.3 V to 2.7 V; V_O = 0.4 V; I_O = 10 mA	7	16	55	
V_{Pass}	Switch output voltage	V_{swin} = V_{DD} = 3.3 V; I_{swout} = –100 µA	—	1.9	—	V
		V_{swin} = V_{DD} = 3.0 V to 3.6 V; I_{swout} = –100 µA	1.6	—	2.8	
		V_{swin} = V_{DD} = 2.5 V; I_{swout} = –100 µA	—	1.5	—	
		V_{swin} = V_{DD} = 2.3 V to 2.7 V; I_{swout} = –100 µA	1.1	—	2.0	
I_L	Leakage current	V_I = V_{DD} or V_{SS}	–1	—	+1	µA
C_{io}	Input/output capacitance	V_I = V_{SS}	—	3	5	pF
$\overline{\text{INT}}$ Output						
I_{OL}	LOW-level output current	V_{OL} = 0.4 V	3	—	—	mA
I_{OH}	HIGH-level output current		—	—	+10	µA

NOTE:
1. V_{DD} must be lowered to 0.2 V in order to reset part.

DC CHARACTERISTICS

V_{DD} = 4.5 V to 5.5 V; V_{SS} = 0 V; T_{amb} = –40 °C to +85 °C; unless otherwise specified. (See page 10 for V_{DD} = 2.3 V to 3.6 V.)

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			MIN	TYP	MAX	
Supply						
V_{DD}	Supply voltage		4.5	—	5.5	V
I_{DD}	Supply current	Operating mode; V_{DD} = 5.5 V; no load; $V_I = V_{DD}$ or V_{SS}; f_{SCL} = 100 kHz	—	25	100	µA
I_{stb}	Standby current	Standby mode; V_{DD} = 5.5 V; no load; $V_I = V_{DD}$ or V_{SS}	—	0.3	1	µA
V_{POR}	Power-on reset voltage (Note 1)	no load; $V_I = V_{DD}$ or V_{SS}	—	1.7	2.1	V
Input SCL; input/output SDA						
V_{IL}	LOW level input voltage		–0.5	—	$0.3V_{DD}$	V
V_{IH}	HIGH level input voltage		$0.7V_{DD}$	—	6	V
I_{OL}	LOW level output current	V_{OL} = 0.4 V	3	—	—	mA
		V_{OL} = 0.6 V	6	—	—	mA
I_L	Leakage current	$V_I = V_{SS}$ or V_{DD}	–1	—	1	µA
C_i	Input capacitance	$V_I = V_{SS}$	—	10	13	pF
Select inputs A0 to A1 / $\overline{\text{INT0}}$ to $\overline{\text{INT3}}$ / $\overline{\text{RESET}}$						
V_{IL}	LOW level input voltage		–0.5	—	$0.3V_{DD}$	V
V_{IH}	HIGH level input voltage		$0.7V_{DD}$	—	V_{DD} + 0.5	V
I_{LI}	Input leakage current	$V_I = V_{DD}$ or V_{SS}	–1	—	+1	µA
C_i	Input capacitance	$V_I = V_{SS}$	—	2	5	pF
Pass Gate						
R_{ON}	Switch resistance	V_{CC} = 4.5 V to 5.5 V, V_O = 0.4 V, I_O = 15 mA	4	9	24	Ω
V_{Pass}	Switch output voltage	$V_{swin} = V_{DD}$ = 5.0 V; I_{swout} = –100 µA	—	3.6	—	V
		$V_{swin} = V_{DD}$ = 4.5 V to 5.5 V; I_{swout} = –100 µA	2.6	—	4.5	V
I_L	Leakage current	$V_I = V_{DD}$ or V_{SS}	–1	—	+1	µA
C_{io}	Input/output capacitance	$V_I = V_{SS}$	—	3	5	pF
$\overline{\text{INT}}$ Output						
I_{OL}	LOW level output current	V_{OL} = 0.4 V	3	—	—	mA
I_{OH}	HIGH level output current		—	—	+10	µA

NOTE:

1. V_{DD} must be lowered to 0.2 V in order to reset part.
2. For operation between published voltage ranges, refer to worse case parameter in both ranges.

AC CHARACTERISTICS

SYMBOL	PARAMETER	STANDARD-MODE I²C-bus		FAST-MODE I²C-bus		UNIT
		MIN	MAX	MIN	MAX	
t_{pd}	Propagation delay from SDA to SD_n or SCL to SC_n	—	0.3[1]	—	0.3[1]	ns
f_{SCL}	SCL clock frequency	0	100	0	400	kHz
t_{BUF}	Bus free time between a STOP and START condition	4.7	—	1.3	—	µs
$t_{HD;STA}$	Hold time (repeated) START condition After this period, the first clock pulse is generated	4.0	—	0.6	—	µs
t_{LOW}	LOW period of the SCL clock	4.7	—	1.3	—	µs
t_{HIGH}	HIGH period of the SCL clock	4.0	—	0.6	—	µs
$t_{SU;STA}$	Set-up time for a repeated START condition	4.7	—	0.6	—	µs
$t_{SU;STO}$	Set-up time for STOP condition	4.0	—	0.6	—	µs
$t_{HD;DAT}$	Data hold time	0[2]	3.45	0[2]	0.9	µs
$t_{SU;DAT}$	Data set-up time	250	—	100	—	ns
t_R	Rise time of both SDA and SCL signals	—	1000	$20 + 0.1C_b$[3]	300	ns
t_F	Fall time of both SDA and SCL signals	—	300	$20 + 0.1C_b$[3]	300	µs
C_b	Capacitive load for each bus line	—	400	—	400	µs
t_{SP}	Pulse width of spikes which must be suppressed by the input filter	—	50	—	50	ns
$t_{VD:DATL}$	Data valid (HL)[4]	—	1	—	1	µs
$t_{VD:DATH}$	Data valid (LH)[4]	—	0.6	—	0.6	µs
$t_{VD:ACK}$	Data valid Acknowledge	—	1	—	1	µs
$\overline{INT}$						
t_{iv}	$\overline{INTn}$ to $\overline{INT}$ active valid time	—	4	—	4	µs
t_{ir}	$\overline{INTn}$ to $\overline{INT}$ inactive delay time	—	2	—	2	µs
L_{pwr}	LOW level pulse width rejection or $\overline{INTn}$ inputs	1	—	1	—	µs
H_{pwr}	HIGH level pulse width rejection or $\overline{INTn}$ inputs	0.5	—	0.5	—	µs
RESET						
$t_{WL(rst)}$	Pulse width low reset	4	—	4	—	ns
t_{rst}	Reset time (SDA clear)	500	—	500	—	ns
$t_{REC:STA}$	Recovery to Start	0	—	0	—	ns

NOTES:
1. Pass gate propagation delay is calculated from the 20 Ω typical R_{ON} and the 15 pF load capacitance.
2. A device must internally provide a hold time of at least 300 ns for the SDA signal (referred to the $V_{IH(min)}$ of the SCL signal) in order to bridge the undefined region of the falling edge of SCL.
3. C_b = total capacitance of one bus line in pF.
4. Measurements taken with 1 kΩ pull-up resistor and 50 pF load.

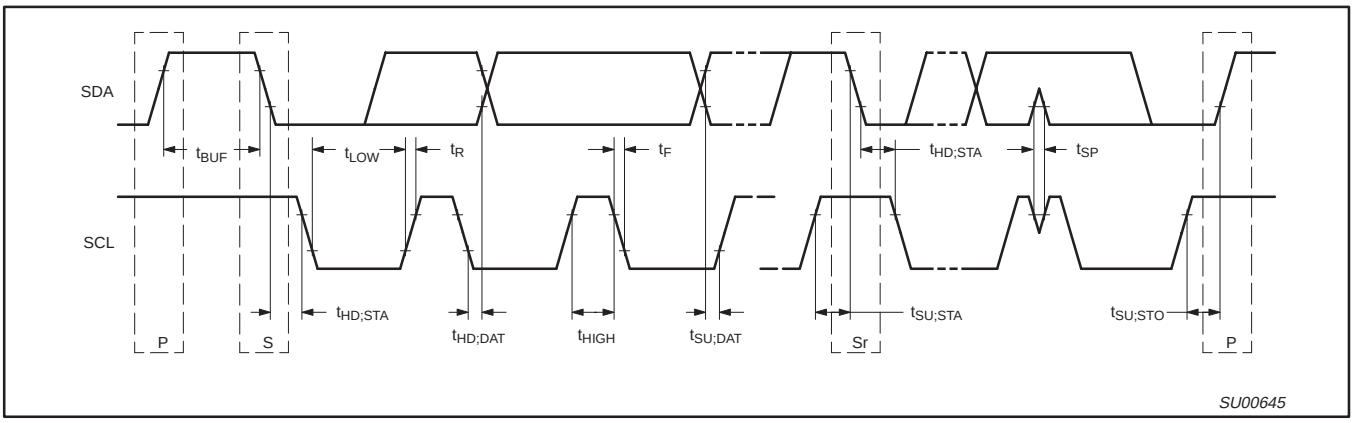


Figure 14. Definition of timing on the I²C-bus

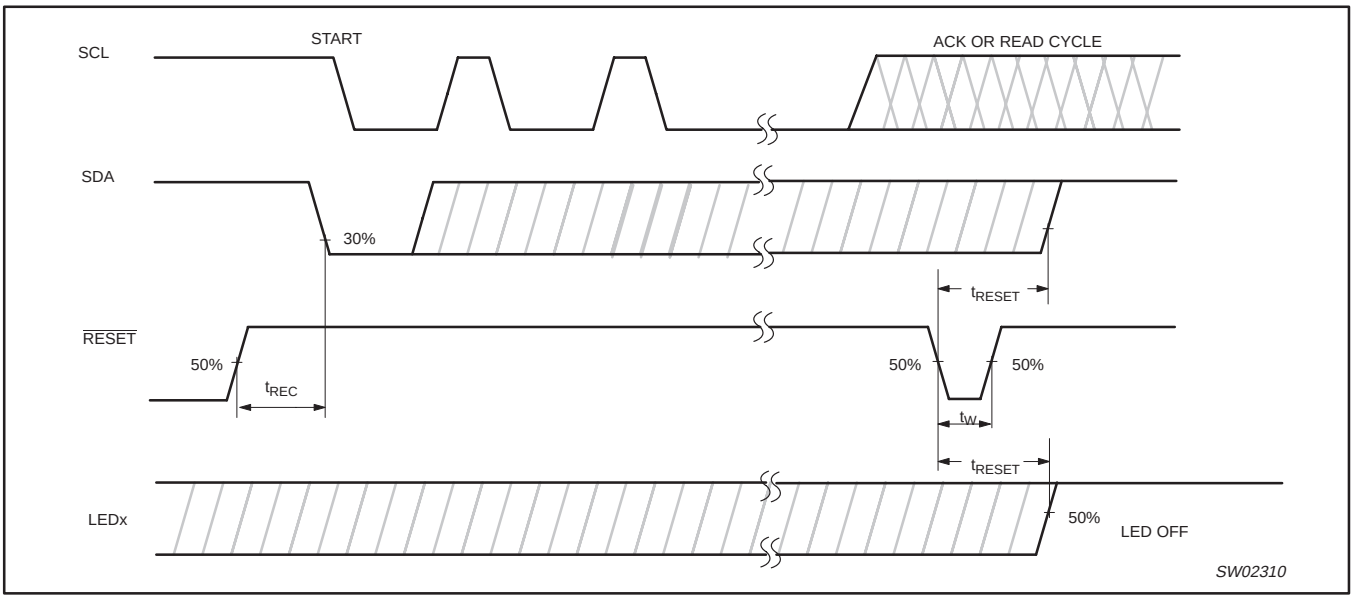


Figure 15. Definition of RESET timing

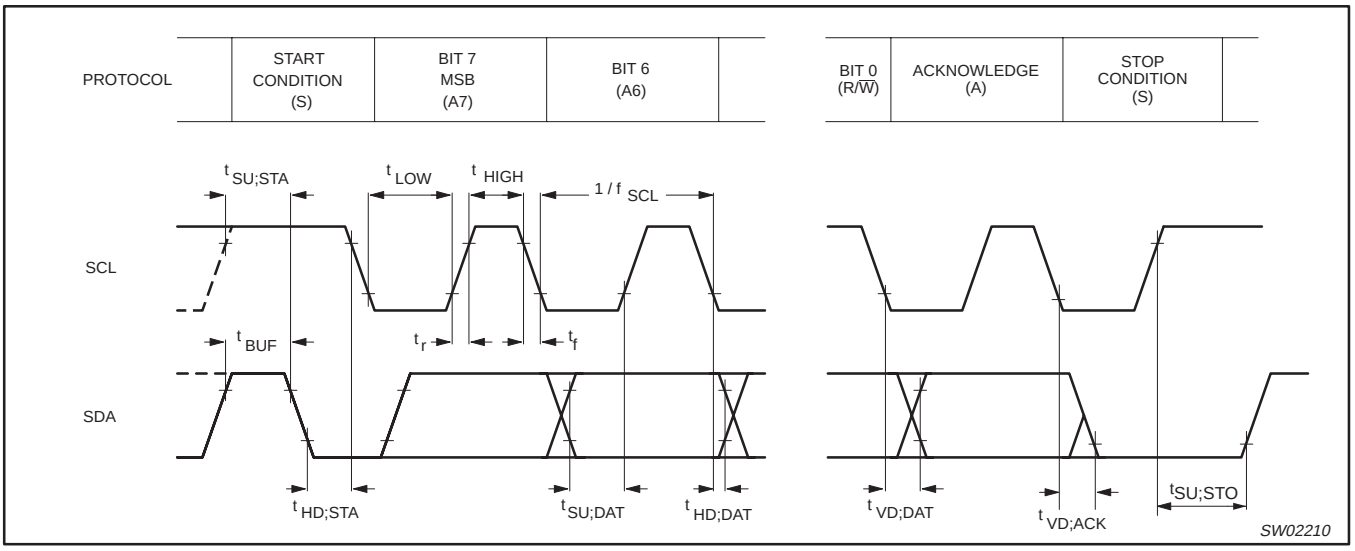


Figure 16. I²C-bus timing diagram; rise and fall times refer to V_{IL} and V_{IH}

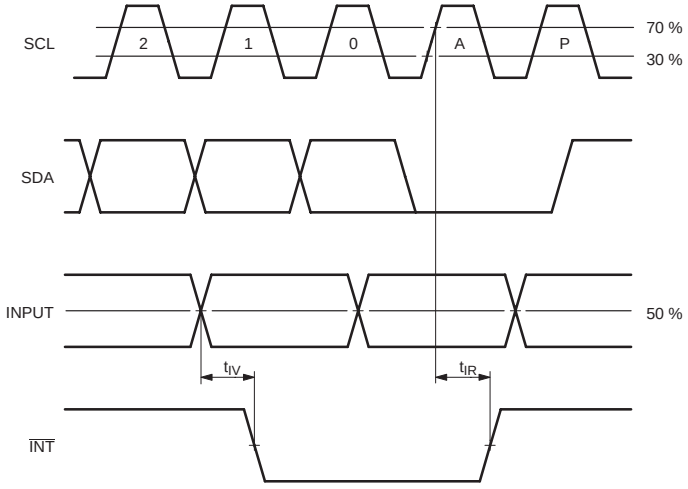
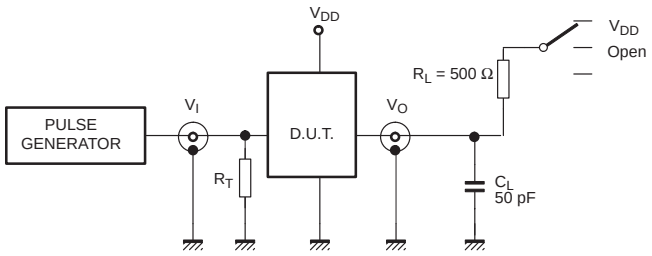


Figure 17. Expanded view of Read input port register

TEST CIRCUITS



DEFINITIONS

R_L = Load resistor.

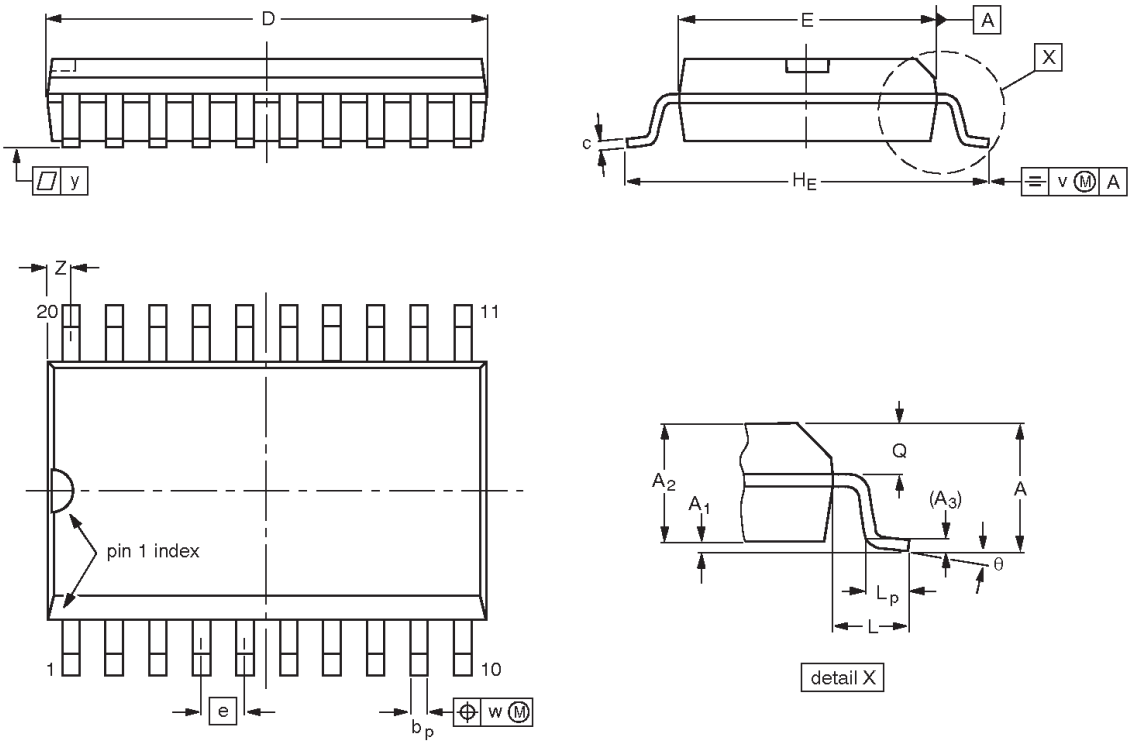
C_L = Load capacitance includes jig and probe capacitance

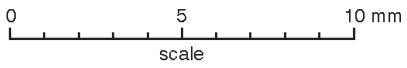
R_T = Termination resistance should be equal to the output impedance Z_O of the pulse generators.

SW02181

Figure 18. Test circuitry for switching times

SO20: plastic small outline package; 20 leads; body width 7.5 mm **SOT163-1**





DIMENSIONS (inch dimensions are derived from the original mm dimensions)

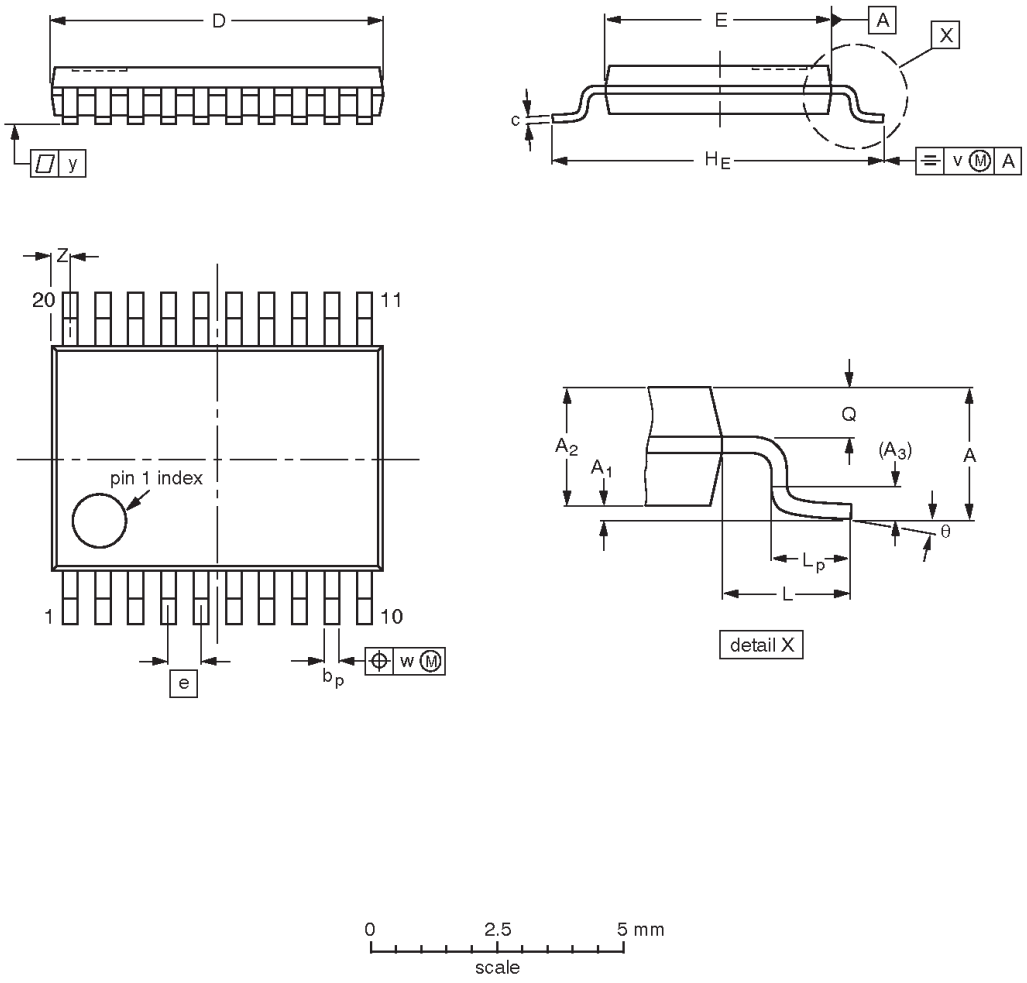
UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	2.65	0.3 0.1	2.45 2.25	0.25	0.49 0.36	0.32 0.23	13.0 12.6	7.6 7.4	1.27	10.65 10.00	1.4	1.1 0.4	1.1 1.0	0.25	0.25	0.1	0.9 0.4	8^o 0^o
inches	0.1	0.012 0.004	0.096 0.089	0.01	0.019 0.014	0.013 0.009	0.51 0.49	0.30 0.29	0.05	0.419 0.394	0.055	0.043 0.016	0.043 0.039	0.01	0.01	0.004	0.035 0.016	

Note

1. Plastic or metal protrusions of 0.15 mm (0.006 inch) maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT163-1	075E04	MS-013				~~99-12-27~~ 03-02-19

TSSOP20: plastic thin shrink small outline package; 20 leads; body width 4.4 mm **SOT360-1**



DIMENSIONS (mm are the original dimensions)

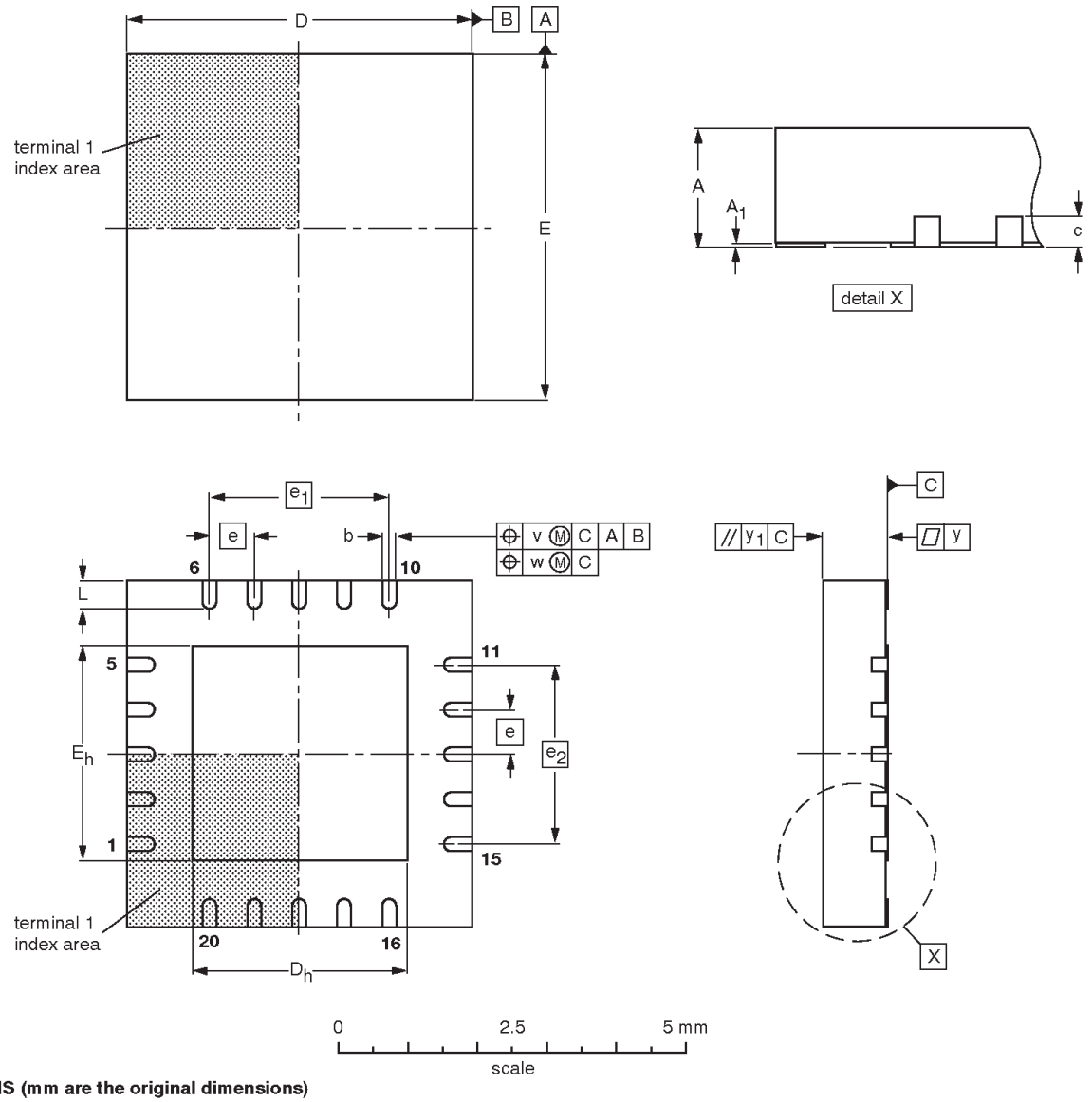
UNIT	A max.	A_1	A_2	A_3	b_p	c	D (1)	E (2)	e	H_E	L	L_p	Q	v	w	y	Z (1)	θ
mm	1.1	0.15 0.05	0.95 0.80	0.25	0.30 0.19	0.2 0.1	6.6 6.4	4.5 4.3	0.65	6.6 6.2	1	0.75 0.50	0.4 0.3	0.2	0.13	0.1	0.5 0.2	8^o 0^o

Notes

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT360-1		MO-153				~~99-12-27~~ 03-02-19

HVQFN20: plastic thermal enhanced very thin quad flat package; no leads; 20 terminals; body 5 x 5 x 0.85 mm **SOT662-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A(1) max.	A_1	b	c	D(1)	D_h	E(1)	E_h	e	e_1	e_2	L	v	w	y	y_1
mm	1	0.05 0.00	0.38 0.23	0.2	5.1 4.9	3.25 2.95	5.1 4.9	3.25 2.95	0.65	2.6	2.6	0.75 0.50	0.1	0.05	0.05	0.1

Note

1. Plastic or metal protrusions of 0.075 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT662-1	- - -	MO-220	- - -			~~01-08-08~~ 02-10-22

REVISION HISTORY

Rev	Date	Description
_2	20040929	**Objective data sheet (9397 750 13989). Supersedes data of 2004 Jul 28 (9397 750 13309).** Modifications: ● Control Register Definition section on page 5: – change third sentence from 'The 2 LSBs of the control byte ...' to 'The 4 LSBs of the control byte ...'. – Table 1. "Control Register; Write — Channel Selection / Read — Channel Status" : add 'No channel selected; power-up/reset default state' row to bottom of table. ● DC characteristics table on page 10: – Description line: change '(See page 11 for V_{DD} = 3.6 V to 5.5 V.)' to '(See page 11 for V_{DD} = 4.5 V to 5.5 V.)' – Supply: change I_{DD} Typ. from 20 μA to 10 μA; change I_{DD} Max. from 50 μA to 30 μA – Input SCL; input/output SDA: change I_{OL} Typ. (V_{OL} = 0.4 V) from '–' to 7 mA change I_{OL} Typ. (V_{OL} = 0.6 V) from '–' to 10 mA change C_i Typ. from 12 pF to 10 pF – $\overline{INT}$ output: change I_{OH} Max. from +100 μA to +10 μA ● DC characteristics table on page 11: – Description line: change 'V_{DD} = 3.6 V to 5.5 V' to 'V_{DD} = 4.5 V to 5.5 V'. – Supply: change V_{DD} Min. from 3.6 V to 4.5 V change I_{DD} Typ. from 65 μA to 25 μA change V_{POR} Typ. from 1.6 V to 1.7 V – Input SCL; input/output SDA: delete symbols I_{IL} and I_{IH} add symbol I_L change C_i Typ. from 12 pF to 10 pF – Select inputs A0 to A1 / $\overline{INT0}$ to $\overline{INT3}$ / $\overline{RESET}$: change I_{LI} Test condition from 'pin at V_{DD} or V_{SS}' to 'V_I = V_{DD} or V_{SS}' change I_{LI} Max. from +50 μA to +1 μA change C_i Typ. from 1.6 pF to 2 pF change C_i Max. from 3 pF to 5 pF – Pass Gate: change I_L Max. from +100 μA to +1 μA – $\overline{INT}$ output: change I_{OH} Max. from +100 μA to +10 μA – Add table note 2. ● AC characteristics table on page 12: Add Note 4 and references to it at parameters $t_{VD;DATL}$ and $t_{VD;DATH}$. ● Add Figures 15, 16, 17 and 18.
_1	20040728	**Objective data sheet (9397 750 13309).**

4-channel I²C switch with interrupt logic and reset PCA9545A

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Date of release: 09-04

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